

JEAN GREY 11.6" Schematic

Stoney Ridge FT4

2019-03-29

REV : A00

DY : None Installed

<Variant Name>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A3

Document Number

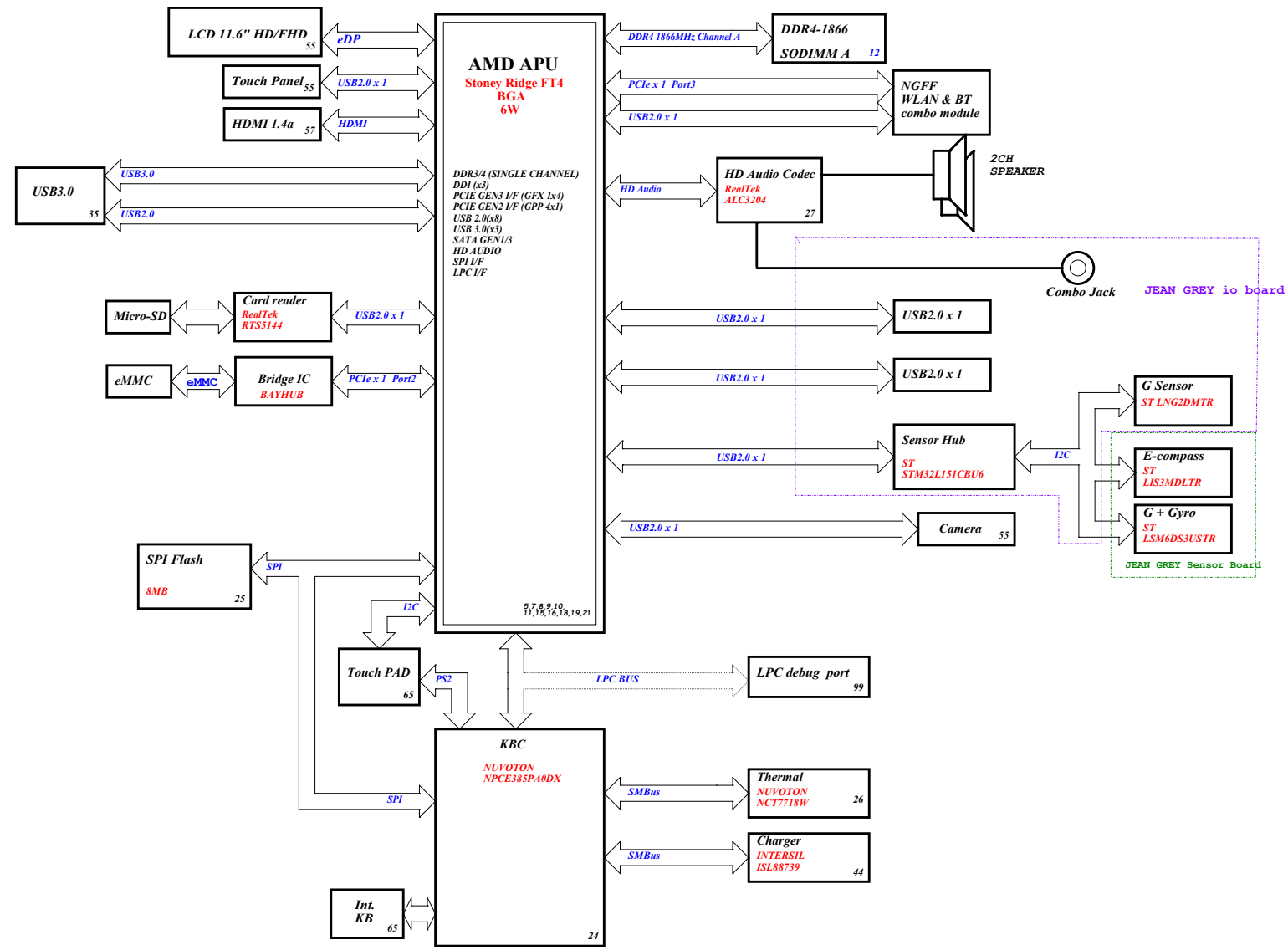
JEAN GREY AMD

Rev
A00

Date: Tuesday, April 02, 2019

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JEAN GREY_AMD Stoney Ridge Block Diagram

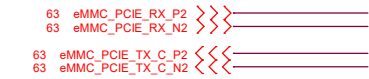


CHARGER		ISL88739HRZ-T	44
INPUTS	OUTPUTS		
AD+ 12V_BT-	DCBATOUT		
SYSTEM DC/DC		RT6575D6QW	45
INPUTS	OUTPUTS		
DCBATOUT	3D3V_AUX_S5	3D3V_S5	5V_AUX_S5
CPU Core Power		ISL62771HRTZ	46-47
INPUTS	OUTPUTS		
DCBATOUT	1V_CPU_CORE	1D2V_CPU_VDDNB	
DDR4 SUS		G5388K11U	53
INPUTS	OUTPUTS		
DCBATOUT	1D2V_S3		
CPU VDDP		G5388K11U	52
INPUTS	OUTPUTS		
DCBATOUT	0D95V_S5		
CPU VDD18		RT5797AL6QW	
		RT9078-18GJ5	54
INPUTS	OUTPUTS		
3D3V_S5	1D8V_S5	1D8V_AUX_S5	
CPU VDDCR6FX		APL5337KAI	49
INPUTS	OUTPUTS		
1D8V_S5	0D775V_S5		
Switches			40
INPUTS	OUTPUTS		
5V_S5	5V_S0		
3D3V_S5	3D3V_S0		
1D8V_S5	1D8V_S0		
0D95V_S5	0D95V_S0		

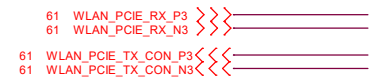
PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

SSID = CPU

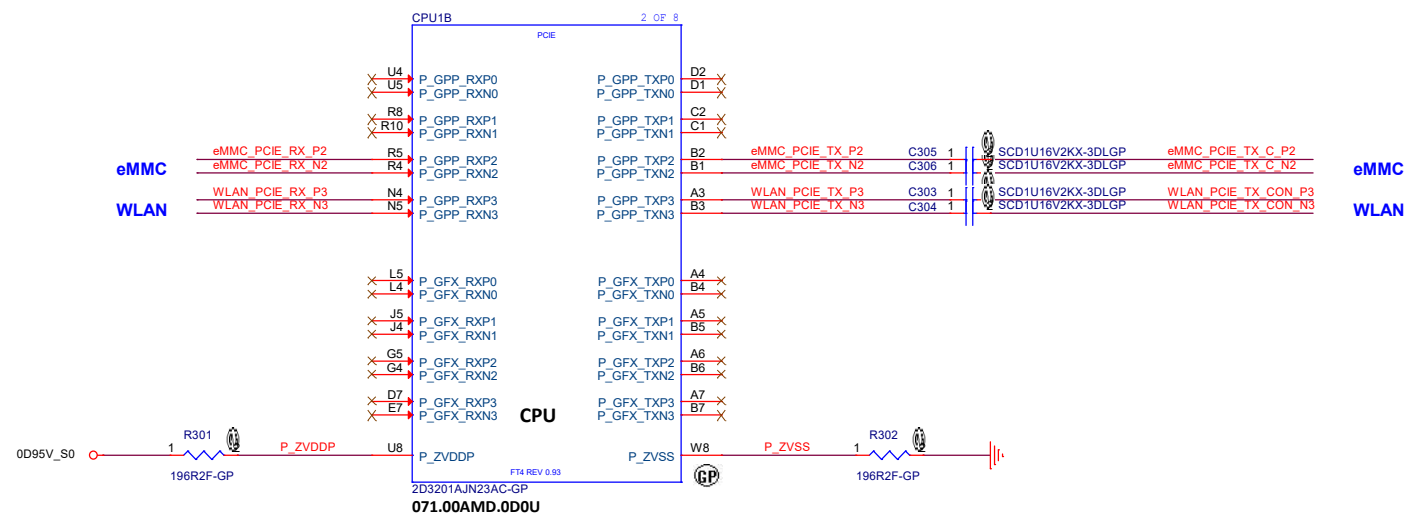
eMMC



WLAN



GPP CLK port	Device	CLKREQ#
2	eMMC	2
3	WLAN	3



SSID = CPU

(Blanking)

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12 DDRA_A_DRAMRST#

12 M_A_EVENT#

12 M_A_CKE0

12 M_A_CKE1

12 M_A_ODT0

12 M_A_ODT1

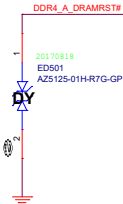
12 M_A_CS#0

12 M_A_CS#1

12 M_A_RAS#

12 M_A_CAS#


12 M_A_WE#



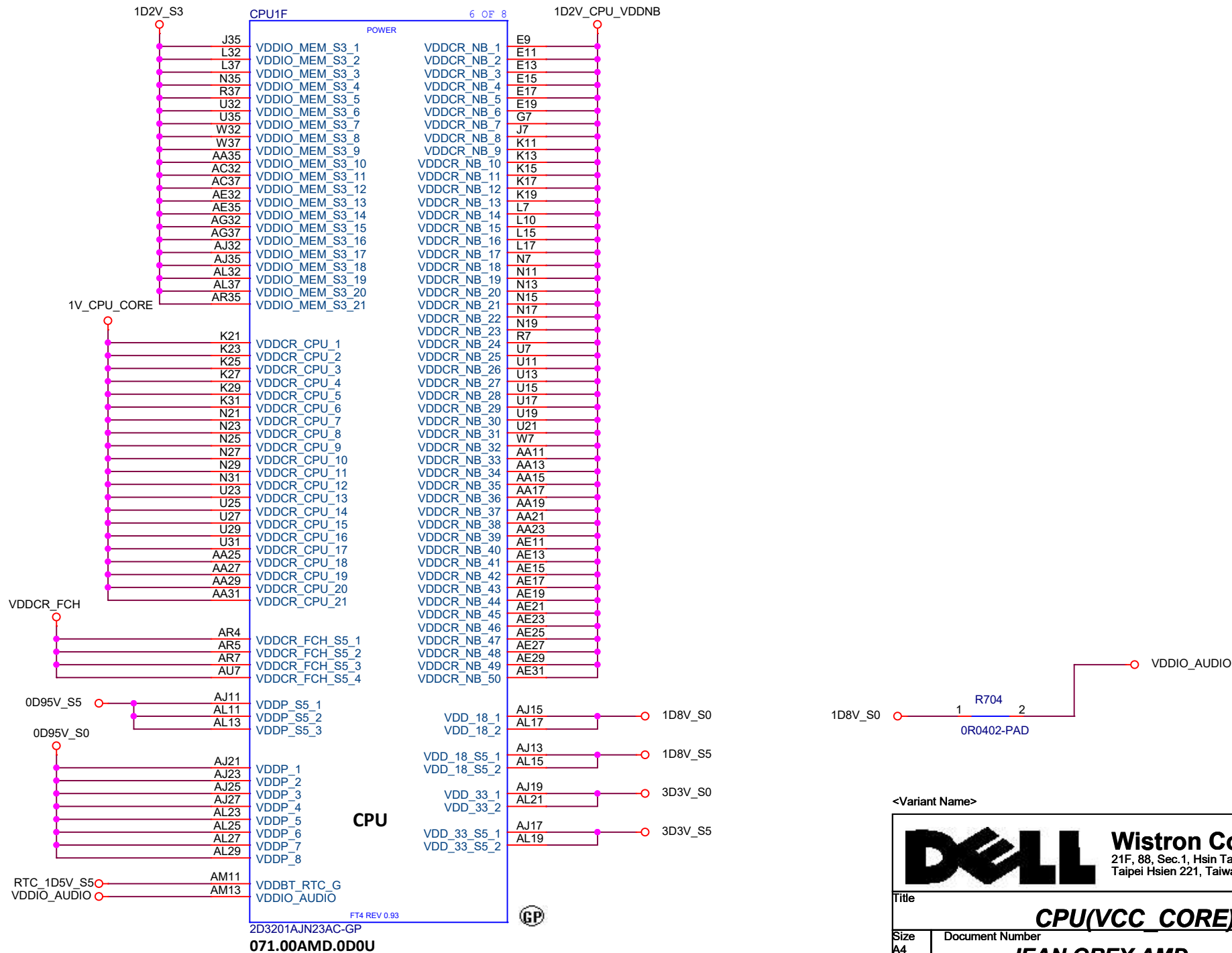
SSID = CPU

(Blanking)

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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SSID = CPU



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Title

CPU(VCC_CORE)

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68 APU_RST_L_BUF    >>>_____
68 APU_PWROK_HDT    <<<_____
68 APU_TEST19_HDT18 <<>>_____
68 APU_TEST18_HDT20 <<>>_____

```

3 OF 8

DP_BLON BL23 eDP_BLON
DP_DIGON B24 LVDS_VDD_EN-CPU
DP_VARY_B1 A24 C-BLT CTRC-CPU

DP_AUX_ZVS8 D21 DP_ZK_ZVS8 R802 150KΩ-1-CP
DP_AUX_ZVS8 B18 DP_ZK_ZVS8 R803 2KΩF-3-CP

G15 eDP_AUX_CPU_P
DP0_AUXP D15 eDP_AUX_CPU_N
DP0_AUXN D15 eDP_HPD_CPO

DP1_AUXP G17 HDMI_SCL_CPU
DP1_AUXN D17 HDMI_SDA_CPU
DP1_HPD D17 HDMI_DET_CPU

G19 X
DP2_AUXP H19 X
DP2_AUXN D19 X
DP2_HPD X

DP0_TXP0 A9 eDP_TX_CPU_P0
DP0_TXN0 B9 eDP_TX_CPU_N0
DP0_TXP1 A10 eDP_TX_CPU_P1
DP0_TXN1 A10 eDP_TX_CPU_N1
DP0_TXP2 B11 A11 X
DP0_TXN2 B11 A12 X
DP0_TXP3 B12 X
DP0_TXN3 X

DP1_TXP0 A14 HDMI_DDI_TX_P2
DP1_TXN0 A14 HDMI_DDI_TX_N2
DP1_TXP1 B15 HDMI_DDI_TX_P1
DP1_TXN1 B15 HDMI_DDI_TX_N1
DP1_TXP2 B16 HDMI_DDI_TX_P0
DP1_TXN2 B16 HDMI_DDI_TX_N0
DP1_TXP3 A17 HDMI_DDI_TX_P3
DP1_TXN3 A17 HDMI_DDI_TX_N3

DP2_TXP0 A19
DP2_TXN0 A20 X
DP2_TXP1 B20 X
DP2_TXN1 A21 X
DP2_TXP2 B21 X
DP2_TXN2 A22 X
DP2_TXP3 B22 X
DP2_TXN3 X

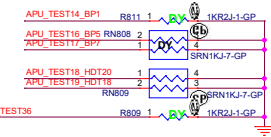
H20 APU_THERMIDA 1 TP801
Q29 APU_THERMIDC 1 TP802
H25 APU_TES16 1 TP803
K32 APU_TES19 1 TP804
N32 APU_TES119 1 TP805
G21 APU_TES14_BPT 1 TP806
H21 APU_TES15_BPT 1 TP807
D23 APU_TES16_BPS 1 TP808
G23 APU_TES117_BPT 1 TP809
A28 APU_TES126_R120 1 TP810
D28 APU_TES128_LD118 1 TP811
N8 APU_TES128_R1 1 TP812
H10 APU_TES128_H 1 TP813
H31 APU_TES131 1 TP814
D25 APU_TES136 1 TP815
B1 APU_TES141 1 TP816

D31 VCCORE_SENSE
E33 VDDNB_SENSE
D35
AMX2
D33 APU_VSS_SENSE_A
AMX3

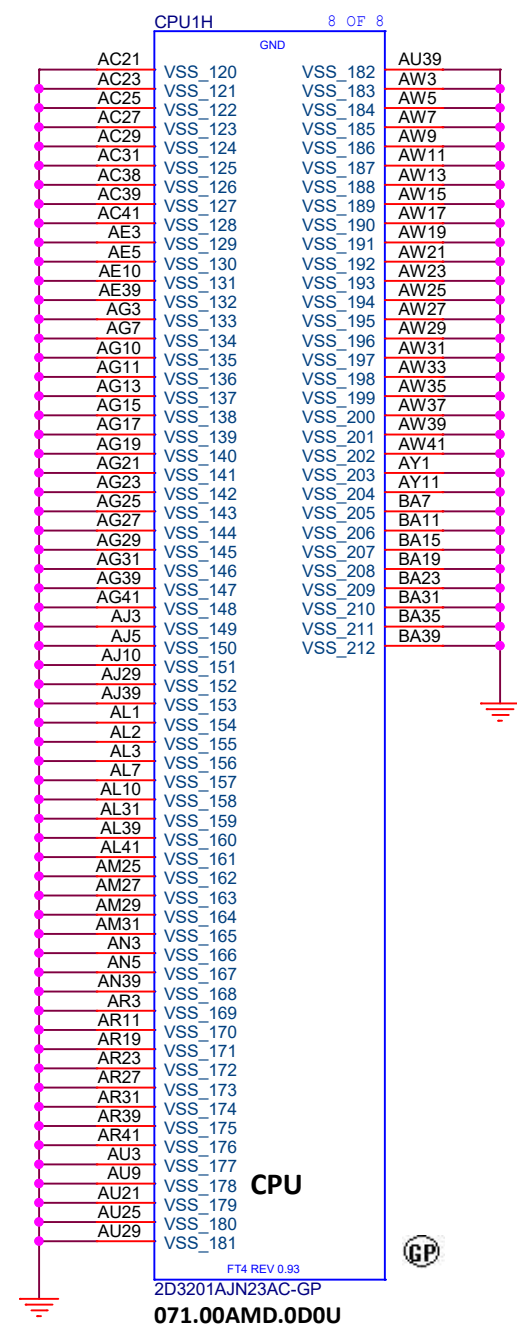
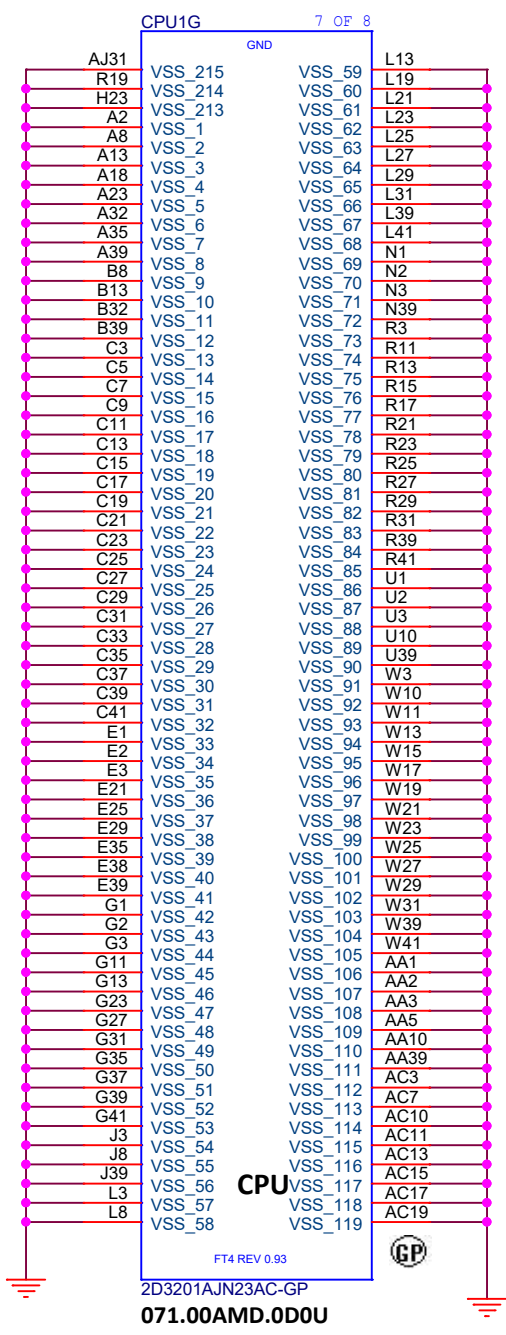
R24 1 2R0402-PAD VSSCORE_SENSE
R25 1 2R0402-PAD VSSNB_SENSE

VSS_VSSENSE_A
VSS_VSSENSE_B


SA



SSID = CPU

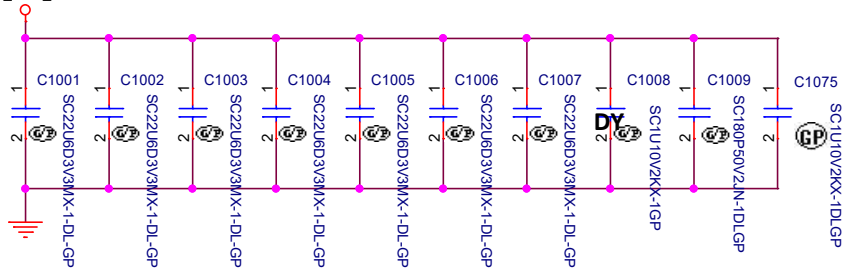


<Variant Name>

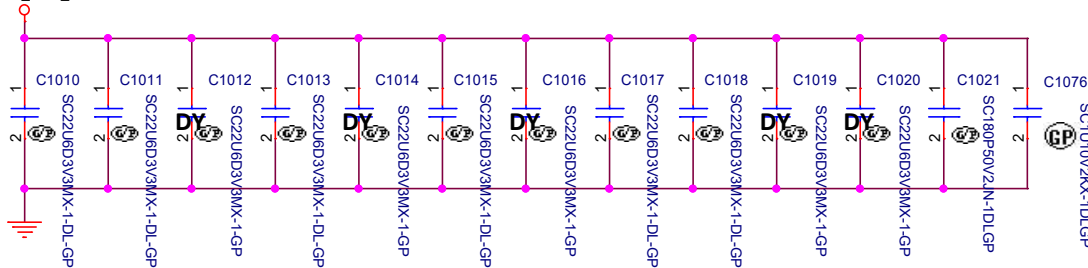
			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CPU (VSS)					
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SSID = CPU

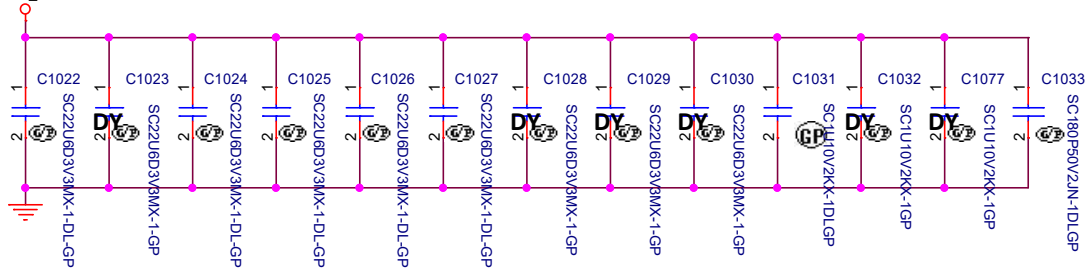
1V_CPU_CORE



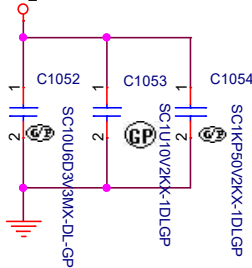
1D2V_CPU_VDDNB



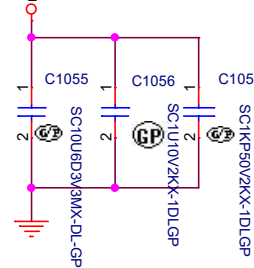
1D2V_S3



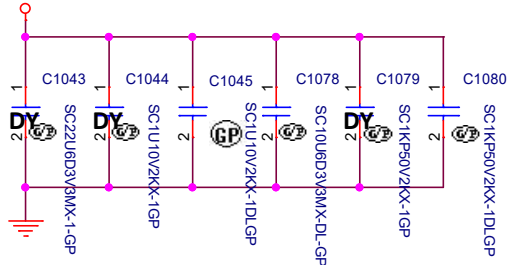
1D8V_S5



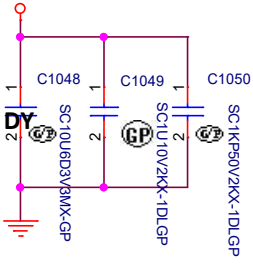
1D8V_S0



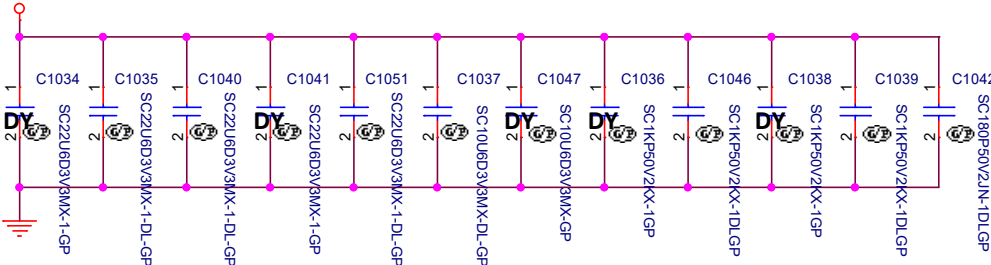
VDDCR_FCH



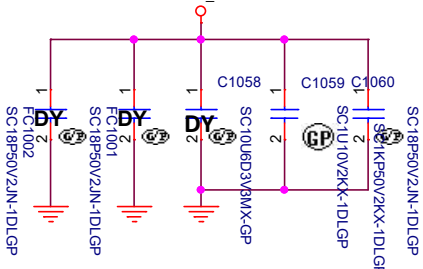
0D95V_S5



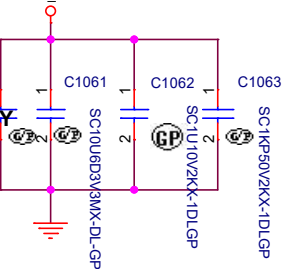
0D95V_S0



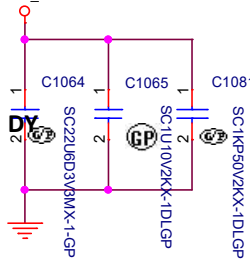
3D3V_S5



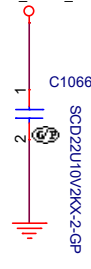
3D3V_S0



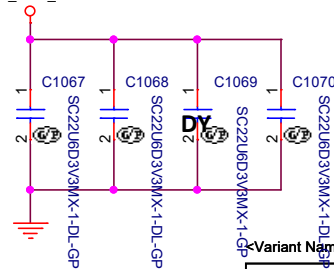
VDDIO_AUDIO



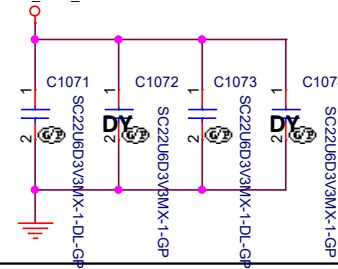
RTC_1D5V_S5




1V_CPU_CORE



1D2V_CPU_VDDNB



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Title		
CPU_(Power CAP1)		
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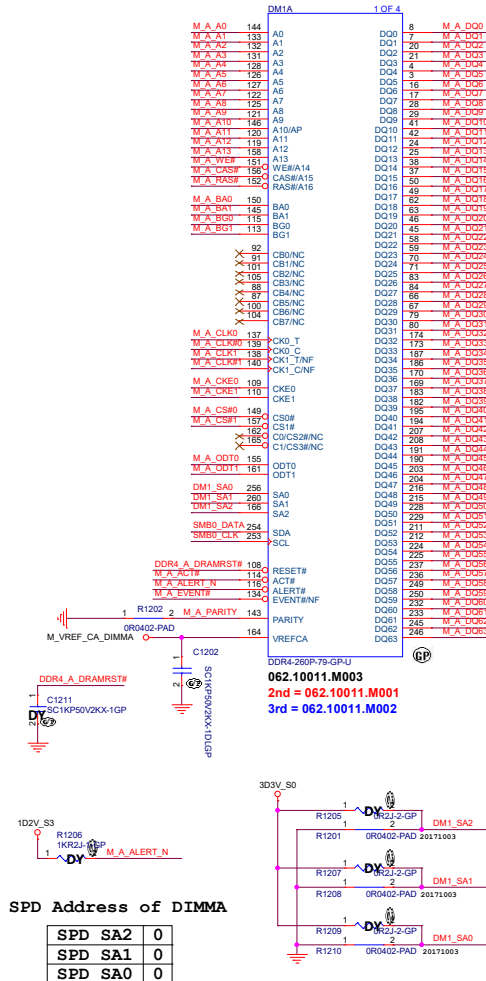
SSID = CPU

(Blanking)

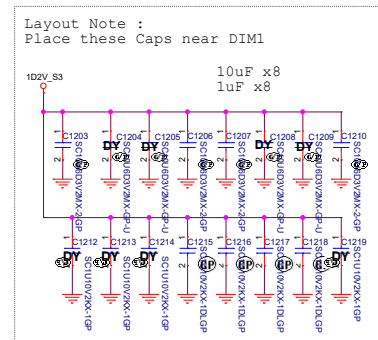
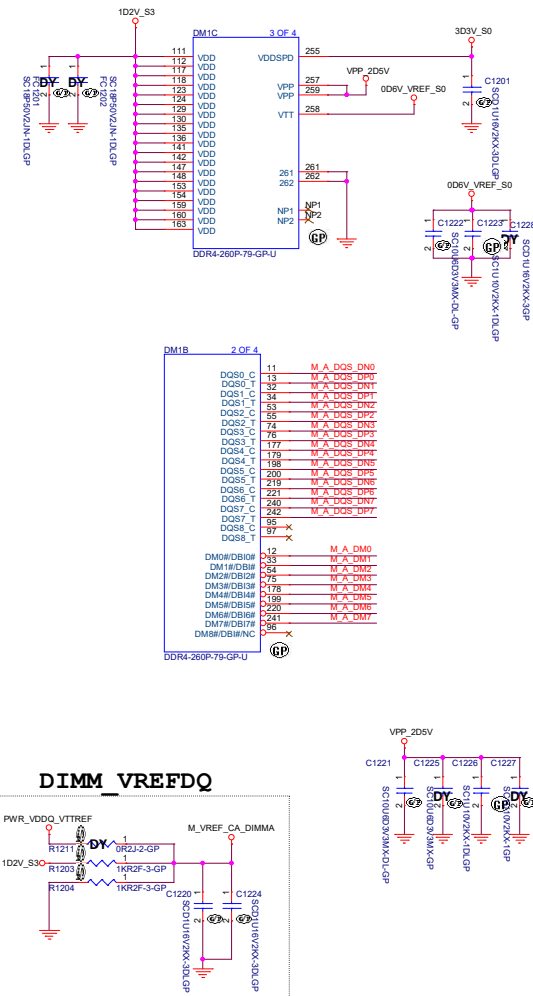
<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)					
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5	M_A_D00		5	M_A_DS_DP0	<<<<
5	M_A_D01		5	M_A_DS_DN0	>>>>
5	M_A_D02				
5	M_A_D03		5	M_A_DS_DP1	<<<<
5	M_A_D04		5	M_A_DS_DN1	>>>>
5	M_A_D05				
5	M_A_D06		5	M_A_DS_DP2	<<<<
5	M_A_D07		5	M_A_DS_DN2	>>>>
5	M_A_D08				
5	M_A_D09				
5	M_A_DQ10		5	M_A_DS_DP3	<<<<
5	M_A_DQ11		5	M_A_DS_DN3	>>>>
5	M_A_DQ12				
5	M_A_DQ13		5	M_A_DS_DP4	<<<<
5	M_A_DQ14		5	M_A_DS_DN4	>>>>
5	M_A_DQ15				
5	M_A_DQ16		5	M_A_DS_DP5	<<<<
5	M_A_DQ17		5	M_A_DS_DN5	>>>>
5	M_A_DQ18				
5	M_A_DQ19		5	M_A_DS_DP6	<<<<
5	M_A_DQ20		5	M_A_DS_DN6	>>>>
5	M_A_DQ21				
5	M_A_DQ22		5	M_A_DS_DP7	<<<<
5	M_A_DQ23		5	M_A_DS_DN7	>>>>
5	M_A_DQ24				
5	M_A_DQ25				
5	M_A_DQ26		5	M_A_DM0	<<<<
5	M_A_DQ27		5	M_A_DM1	>>>>
5	M_A_DQ28		5	M_A_DM2	<<<<
5	M_A_DQ29		5	M_A_DM3	>>>>
5	M_A_DQ30		5	M_A_DM4	<<<<
5	M_A_DQ31		5	M_A_DM5	>>>>
5	M_A_DQ32		5	M_A_DM6	<<<<
5	M_A_DQ33		5	M_A_DM7	>>>>
5	M_A_DQ34				
5	M_A_DQ35				
5	M_A_DQ36				
5	M_A_DQ37				
5	M_A_DQ38				
5	M_A_DQ39				
5	M_A_DQ40				
5	M_A_DQ41				
5	M_A_DQ42				
5	M_A_DQ43				
5	M_A_DQ44				
5	M_A_DQ45				
5	M_A_DQ46				
5	M_A_DQ47				
5	M_A_DQ48				
5	M_A_DQ49				
5	M_A_DQ50				
5	M_A_DQ51				
5	M_A_DQ52				
5	M_A_DQ53				
5	M_A_DQ54				
5	M_A_DQ55				
5	M_A_DQ56				
5	M_A_DQ57				
5	M_A_DQ58				
5	M_A_DQ59				
5	M_A_DQ60				
5	M_A_DQ61				
5	M_A_DQ62				
5	M_A_DQ63				



SPD	SA2	0
SPD	SA1	0
SPD	SA0	0



Layout Note :
Place these Caps near DIM1

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A

<Variant Name>

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Title (Reserved)					
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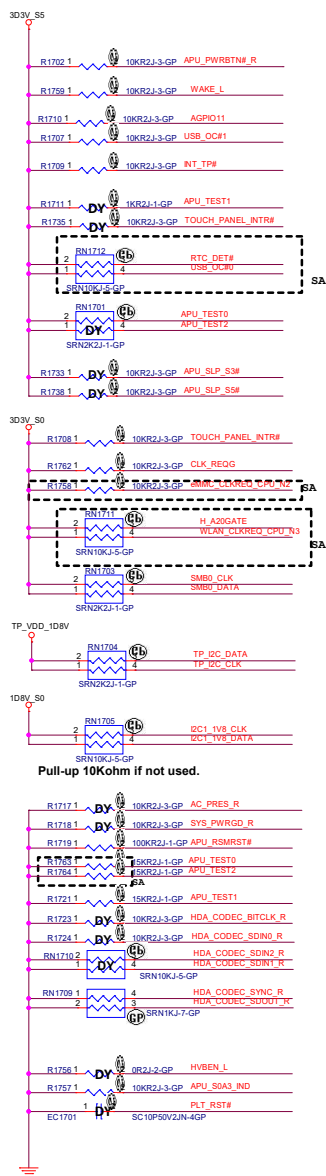
(Blanking)

<Variant Name>

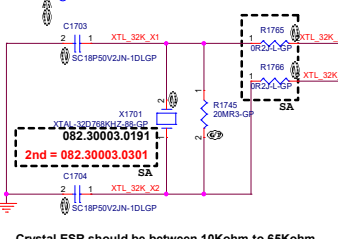
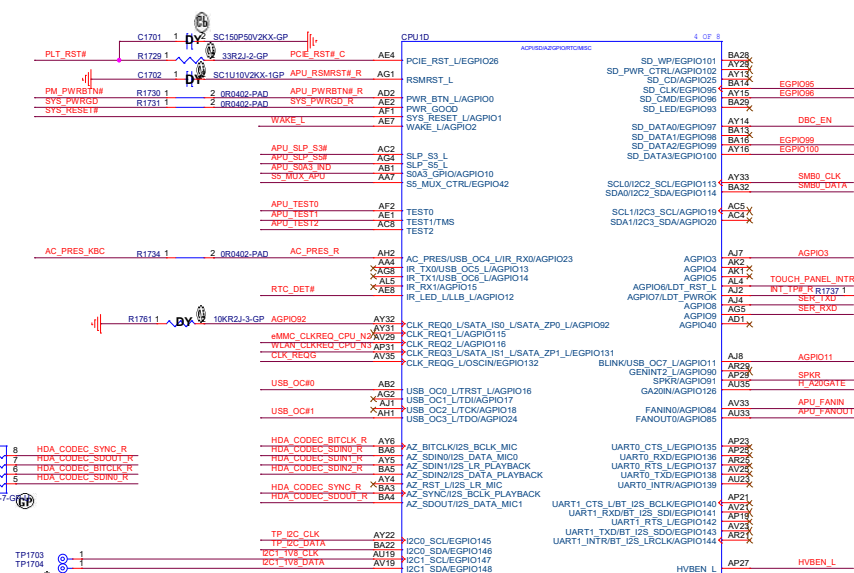
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
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SSID = CPU

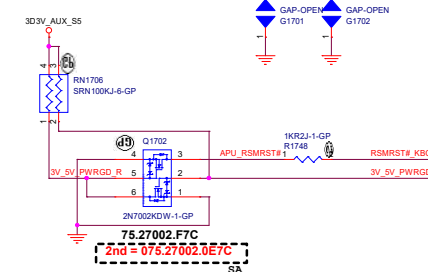
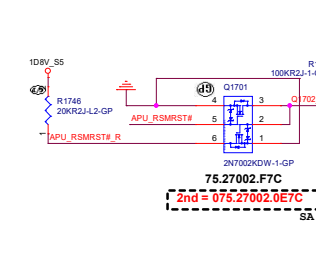
- 61.63.68 PLT_RST# <<<
- 20 SYS_RESET# <<<
- 24 PM_PWRBTN# >>>
- 24.26.40 SYS_PWRGD >>>
- 24.40.53 APU_SLP_S3# <<<
- 24.44.53 APU_SLP_S5# <<<
- 40 SS_MUX_APU <<<
- 24 AC_PRES_KBC >>>
- 25 RTC_DET# >>>
- 63 eMMC_CLKREQ_CPU_N2 >>>
- 61 WLAN_CLKREQ_CPU_N3 >>>
- 66 USB_OC#0 >>>
- 36 USB_OC#1 >>>
- 27 HDA_SYNC_CODEEC <<<
- 27 HDA_SDOUT_CODEEC <<<
- 27 HDA_BITCLK_CODEEC <<<
- 27 HDA_SDIN0_CPU >>>
- 65 TP_OC_CLK <<<
- 65 TP_OC_DATA <<<
- 24 RSMRST#_KBC >>>
- 46.48.54 3V_5V_PWRGD >>>
- 55 DBC_EN <<<
- 12 SMBD_CLK <<<
- 12 SMBD_DATA <<<
- 20 AGPIO3 <<<
- 25.55 TOUCH_PANEL_INTR# >>>
- 65 INT_TP# >>>
- 61 SER_TXD <<<
- 61 SER_RXD >>>
- 27 SPKR <<<
- 24 H_A20GATE >>>
- 20 RTC_CLK <<<



Pull-up 10Kohm if not used.



Crystal ESR should be between 10Kohm to 65Kohm.



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File: CPU(AZ/SD/AG/GPIO/RTC)

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<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
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<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
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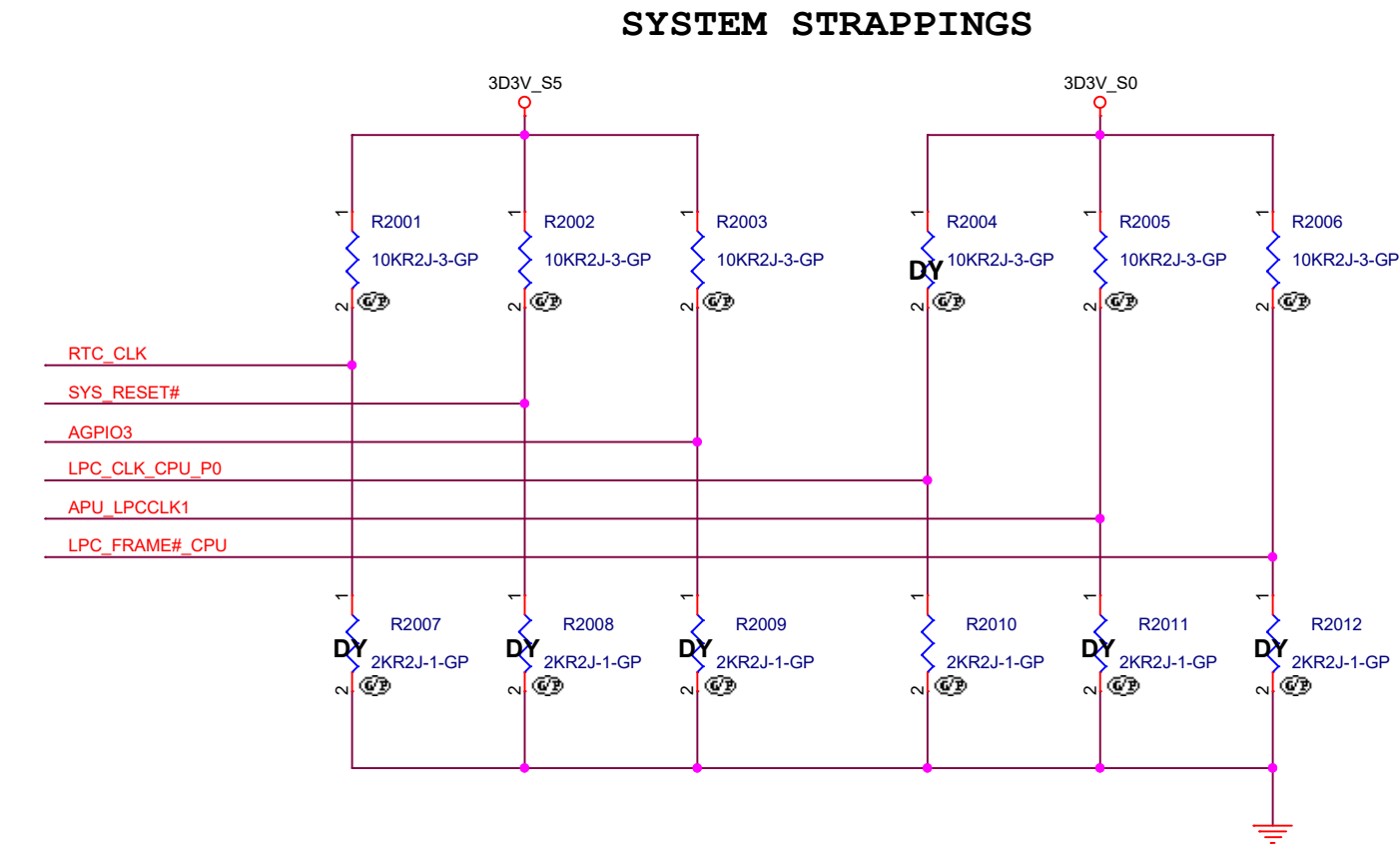
3

2

1

SSID = STRAPING


- 17 RTC_CLK <<<---
- 17 SYS_RESET# <<<---
- 17 AGPIO3 <<<---
- 16,24 LPC_CLK_CPU_P0 <<<---
- 16 APU_LPCCLK1 <<<---
- 16,24,68 LPC_FRAME#_CPU <<<---



REQUIRED SYSTEM STRAPS

	RTC_CLK	SYS_RESET#	AGPIO3	LPC_CLK0	LPC_CLK1	LPC_FRAME#
Type	I	I	I	II	II	II
PULL HIGH	RTC Coin Battery is implemented DEFAULT	NORMAL POWR UP /RESET TIMING DEFAULT	Enhanced Reset logic DEFAULT	Boot Fail Timer Enabled	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT
PULL LOW	RTC Coin Battery is not implemented	Reserved	Traditional Reset logic	Boot Fail Timer Disabled DEFAULT	Reserved	LPC ROM

<Variant Name>



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Title

CPU_Strappings

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(Blanking)

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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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(Blanking)

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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(Blanking)

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)					
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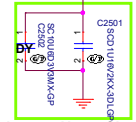
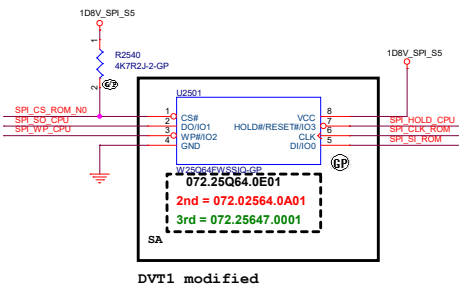
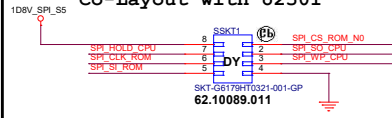
SSID = Flash.ROM

16 SPI_HOLD_CPU >>> _____
16,24 SPI_CLK_ROM >>> _____
16,24 SPI_SI_ROM >>> _____
16,24 SPI_CS_ROM_N0 >>> _____
16,24 SPI_SO_CPU <<< _____
16 SPI_WP_CPU <<< _____
40 1D8V_S0_EN >>> _____

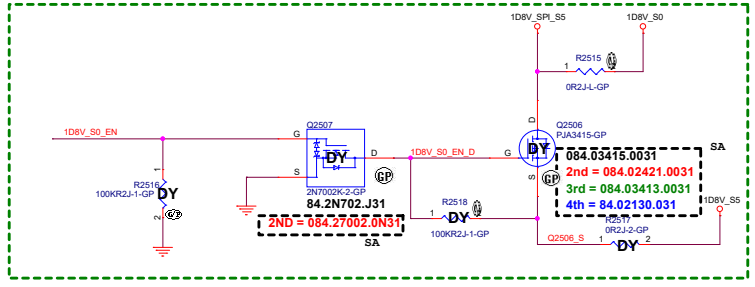
SPI FLASH ROM (8M byte) for CPU

DVT1 modified

SPI ROM socket
Co-Layout with U2501

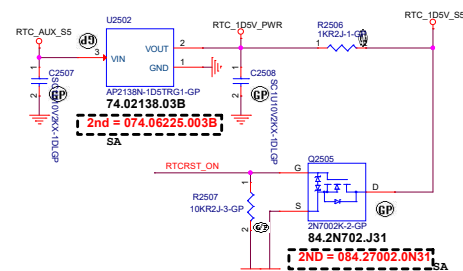
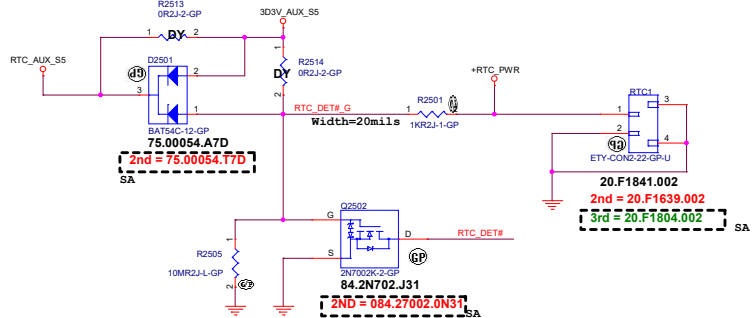


Layout Note: Close to U2501 Pin 8




SSID = RTC

17 RTC_DET# <<< _____
24 RTCRST_ON >>> _____




<Variant Name>

[illegible]

Layout Note: 
Tied at point only under
Codec or near the Codec

Blanking

<Variant Name>

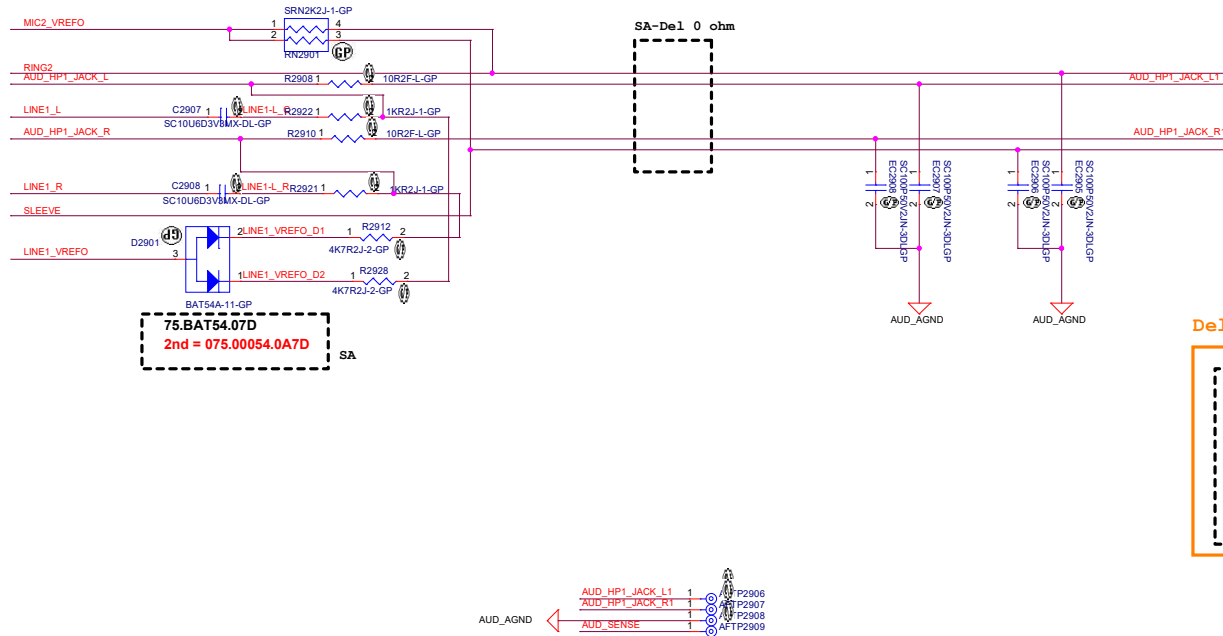
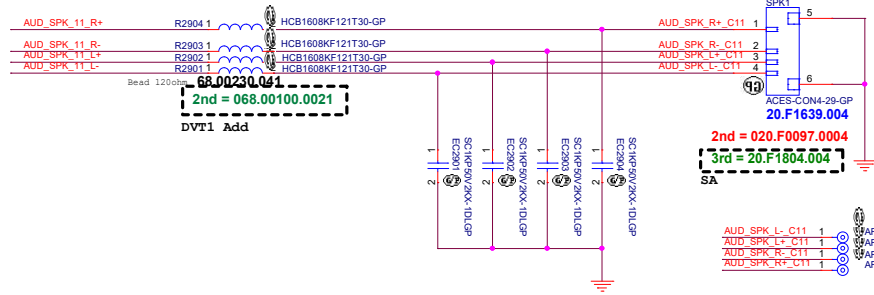
			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)					
Size	Document Number				Rev
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SSID = AUDIO

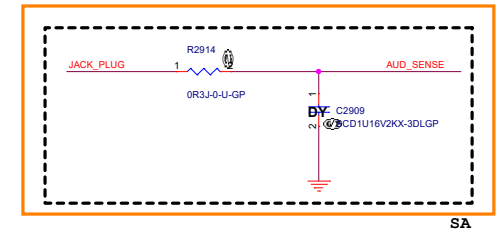
27 AUD_SPK_11_R+ >>>
27 AUD_SPK_11_R- >>>
27 AUD_SPK_11_L+ >>>
27 AUD_SPK_11_L- >>>

27 MIC2_VREF0 >>>
27 RING2 <<<
27 AUD_HP1_JACK_L >>>
27 LINE1_L <<<
27 AUD_HP1_JACK_R >>>
27 LINE1_R <<<
27 SLEEVE <<<
27 LINE1_VREF0 >>>
27 AUD_SENSE <<<

66 JACK_PLUG >>>
66 RING2 >>>
66 AUD_HP1_JACK_L1 <<<
66 AUD_HP1_JACK_R1 <<<
66 SLEEVE >>>



Delay circuit



<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title
Speaker/HPMIC CONN
Size Custom Document Number **JEAN GREY AMD** Rev **A00**
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Blanking

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)LOM			
Size A4	Document Number JEAN GREY AMD		Rev A00
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Blanking

<Variant Name>

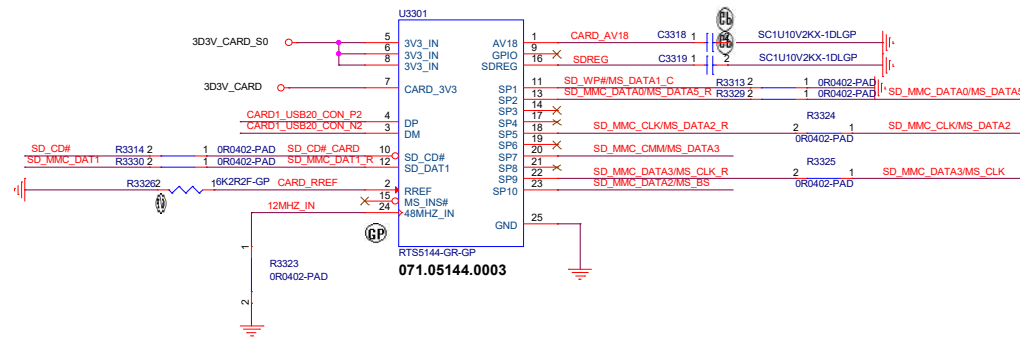
			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title (Reserved)LAN					
Size A4	Document Number JEAN GREY AMD				Rev A00
Date: Tuesday, April 02, 2019			Sheet 31 of 109		

Blanking

<Variant Name>

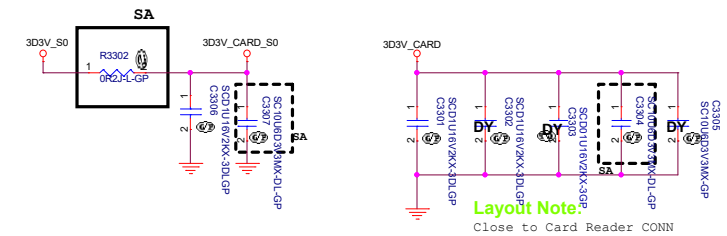
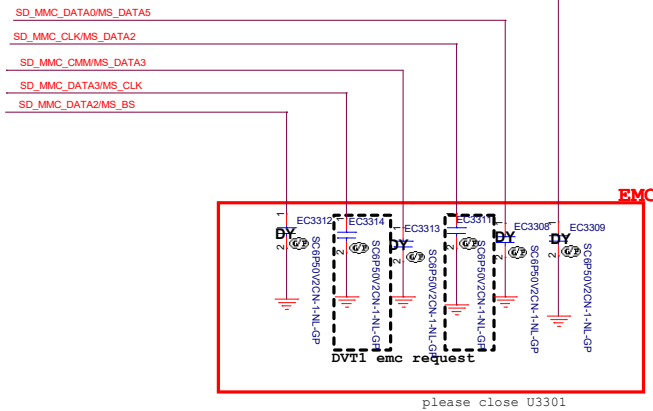
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title (Reserved)RJ45+Transformer		
Size A4	Document Number JEAN GREY AMD	Rev A00
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16 CARD1_USB20_P2 <<>>
16 CARD1_USB20_N2 <<>>

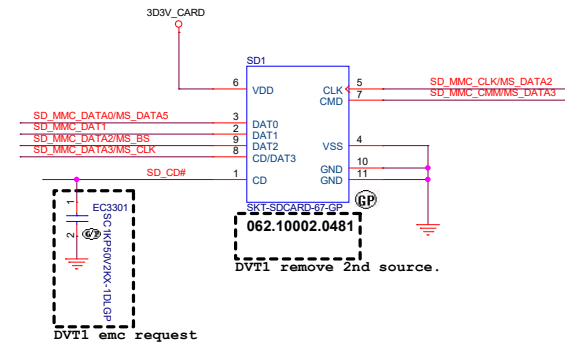


Net name	
Pin name	
SD_DAT1	SD_MMC_DAT1
SP1	SD_WP/MS_DATA1
SP2	SD_MMC_DATA0/MS_DATA5
SP3	MMC_DATA7/MS_DATA4
SP4	MMC_DATA6/MS_DATA0
SP5	SD_MMC_CLK/MS_DATA2
SP6	MMC_DATA5/MS_DATA6
SP7	SD_MMC Command/MS_DATA3
SP8	MMC_DATA4/MS_DATA7
SP9	SD_MMC_DATA3/MS_CLK
SP10	SD_MMC_DATA2/MS_BS

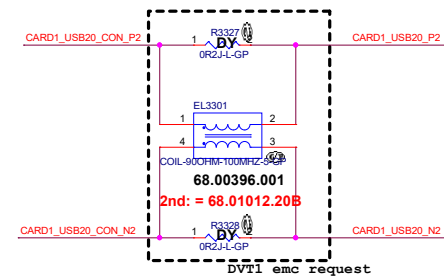
SD_MMC_DAT1



Layout Note:
Close to Card Reader CONN



Pin Define	
P1	SWITCH TERM CD
P2	DAT1
P3	DAT0
P4	VSS
P5	CLK
P6	VDD
P7	CMD
P8	CD/DAT3
P9	DAT2
P10	GND
P11	GND



<Variant Name>




Title	Card Reader + CONN
-------	---------------------------

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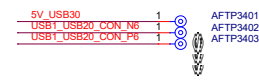
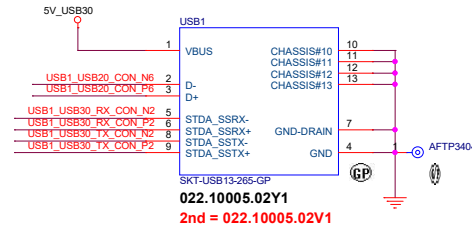
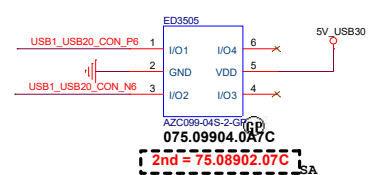
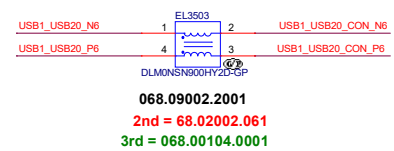
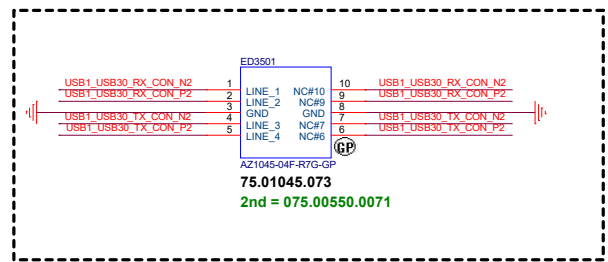
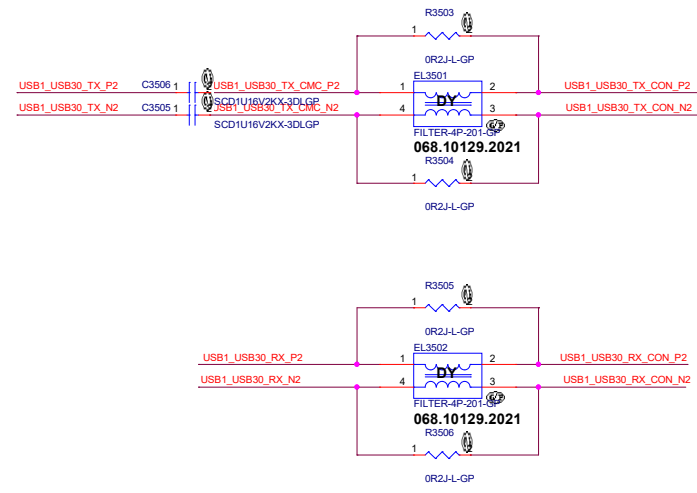
Blanking

<Variant Name>

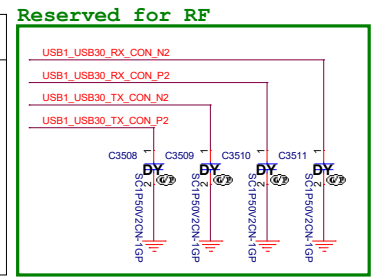
			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)USB 2.0 Port					
Size		Document Number			Rev
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SSID = USB

16 USB1_USB30_TX_P2 >>>>
16 USB1_USB30_TX_N2 >>>>
16 USB1_USB30_RX_P2 <<<<
16 USB1_USB30_RX_N2 <<<<
16 USB1_USB20_P6 <<<<
16 USB1_USB20_N6 <<<<



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



<Variant Name>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB3.0 CONN**

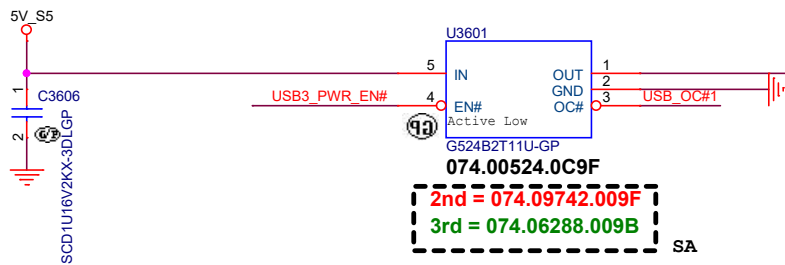
Size: Document Number: **JEAN GREY AMD** Rev: **A00**

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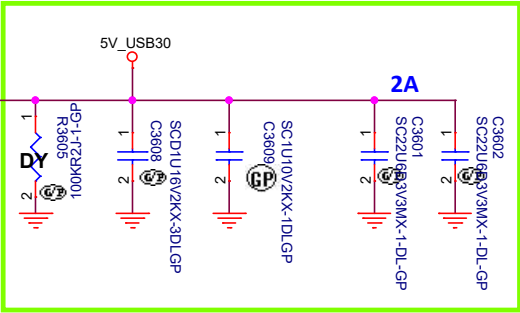
SSID = USB

24 USB3_PWR_EN# >>>—
17 USB_OC#1 <<<—


USB3.0 Port1



Layout Note: Close CON1




<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title USB Power SW			
Size Custom	Document Number JEAN GREY AMD		Rev A00
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Blanking

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB2.0 HUB			
Size	Document Number		Rev
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Blanking

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)					
Size	Document Number				Rev
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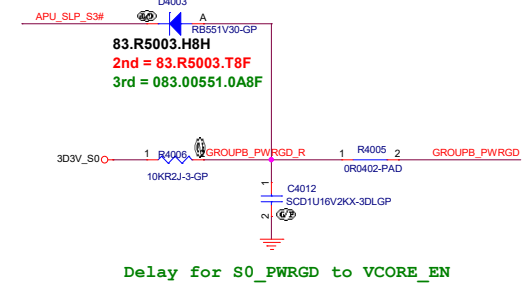
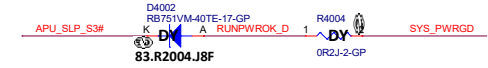
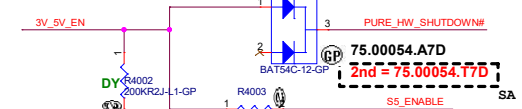
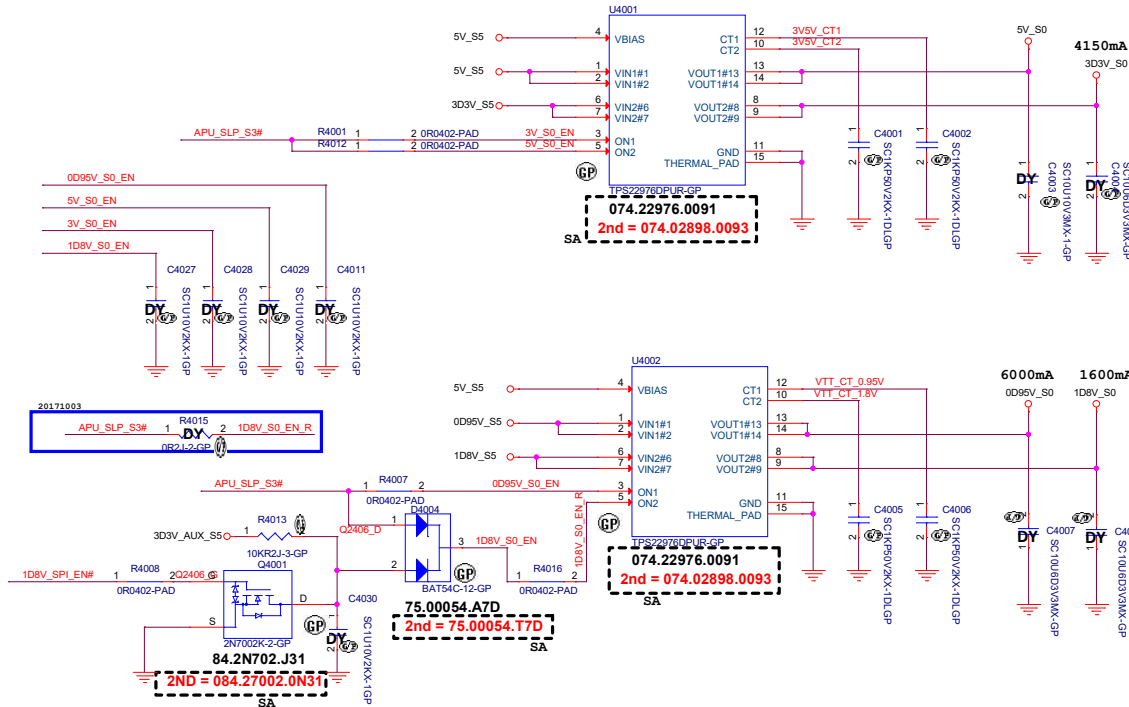
Blanking

<Variant Name>

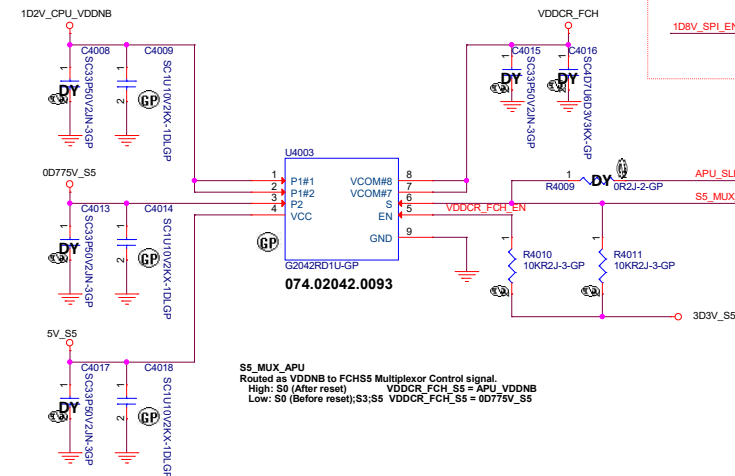
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number JEAN GREY AMD		Rev A00
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Power Sequence

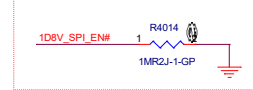
17,24,53 APU_SLP_S3# >>>
25 1D8V_S0_EN >>>
24 1D8V_S1_EN# >>>
17 S5_MUX_APU <<<
45 3V_S5_EN <<<
24,26 PURE_HW_SHUTDOWN# >>>
24 S5_ENABLE >>>
17,24,26 SYS_PWRGD <<<
46 GROUPB_PWRGD <<<



VDDNB to FCHS5 Multiplexor Control signal



DVT2: Add 1M ohm Pull-down on 1D8V_S1_EN# 7/18



VCC	EN	S	P1 Voltage	Function
5	0	X	X	Both P1 and P2 do not pass to VCOM. VCOM is with pull low R of 200 Ω
5	1	0	< P2	P2 passed to VCOM
5	1	0	> P2	P1 passed to VCOM
5	1	1	< 2.0V	P1 passed to VCOM

"X" means don't care

Table 148. S5_MUX_CTRL State Table

Platform Power State	S5_MUX_CTRL Signal Level	SLP_S3_L	SLP_S5_L	VDDCR_FCH_S5 Voltage
G3	X	0	0	OFF
S5	0	0	0	ON (= VDDCR_FCH_ALW)
S3	0	0	1	ON (= VDDCR_FCH_ALW)
S0, but still in Reset	0	1	1	ON (= VDDCR_FCH_ALW) or if VDDCR_NB ≥ VDDCR_FCH_ALW, tracks VDDCR_NB
S0	1	1	1	Tracks VDDCR_NB

<Variant Name>

DELL Wistron Corporation
21F, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

Title: **Power Plane Enable&Sequence**

Size: Custom Document Number: **JEAN GREY AMD** Rev: **A00**

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5

4

3

2

1

D

D

C

C

B


B

A

A

(Blanking)

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title (Reserved)					
Size A4	Document Number JEAN GREY AMD				Rev A00
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5

4


3

2

1

Blanking

<Variant Name>

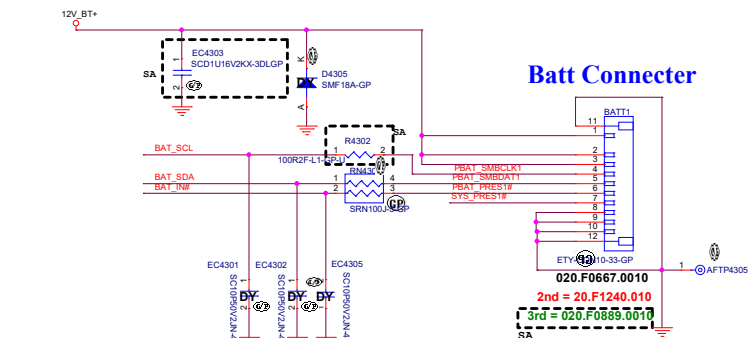
			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title (Reserved)					
Size A4		Document Number JEAN GREY AMD			Rev A00
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```
SSID = PWR.Support
```

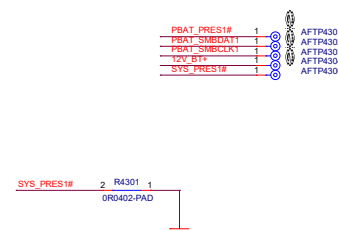
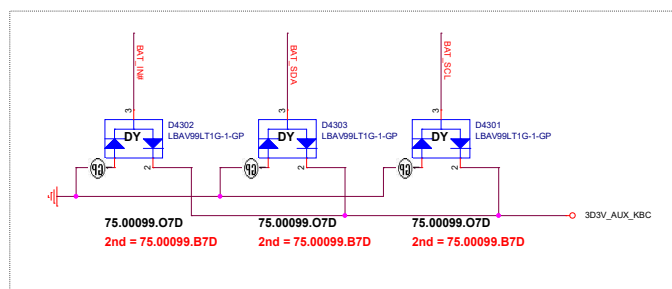
```

24,44 BAT_SCL <<<>>>_____
24,44 BAT_SDA <<<>>>_____
24,44 BAT_IN# <<<_____
24,44 PWR_CHG_AD_OFF >>>_____
24 PSID_EC <<<_____

```



Placement: Close to Batt Connector



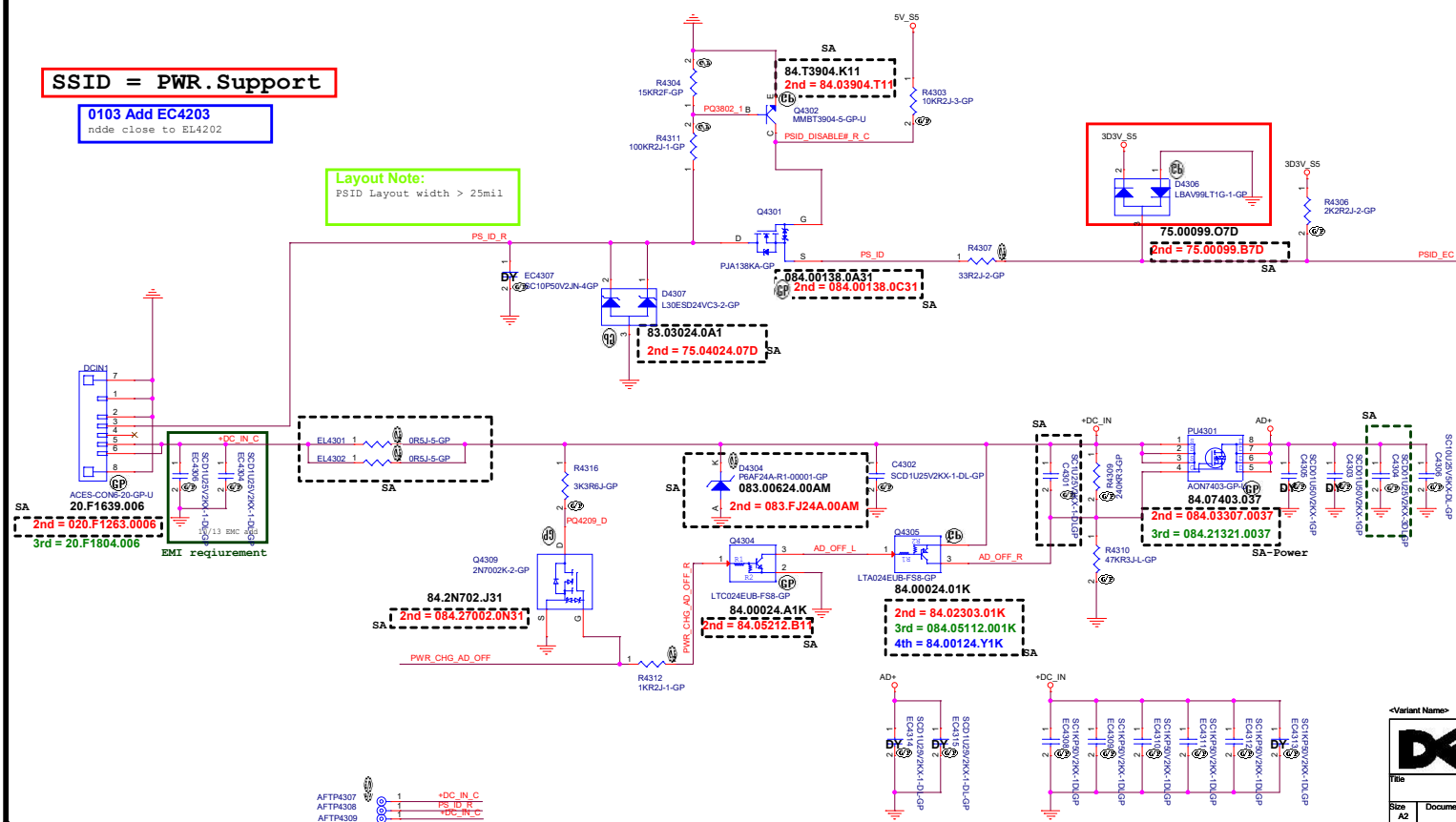
```
SSID = PWR.Support
```

0103 Add EC4203

ndde close to EL4202

Layout Note:

PSID Layout width > 25mil



<Variant Name>

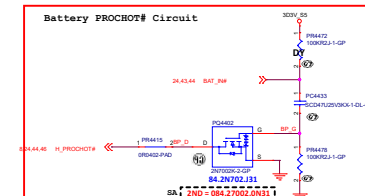
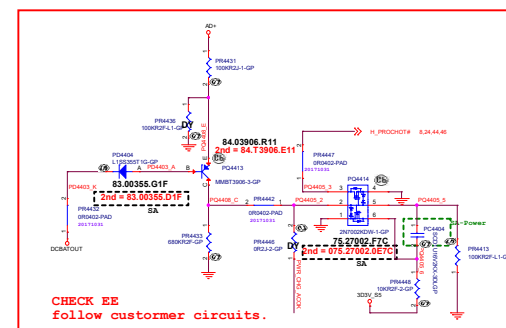
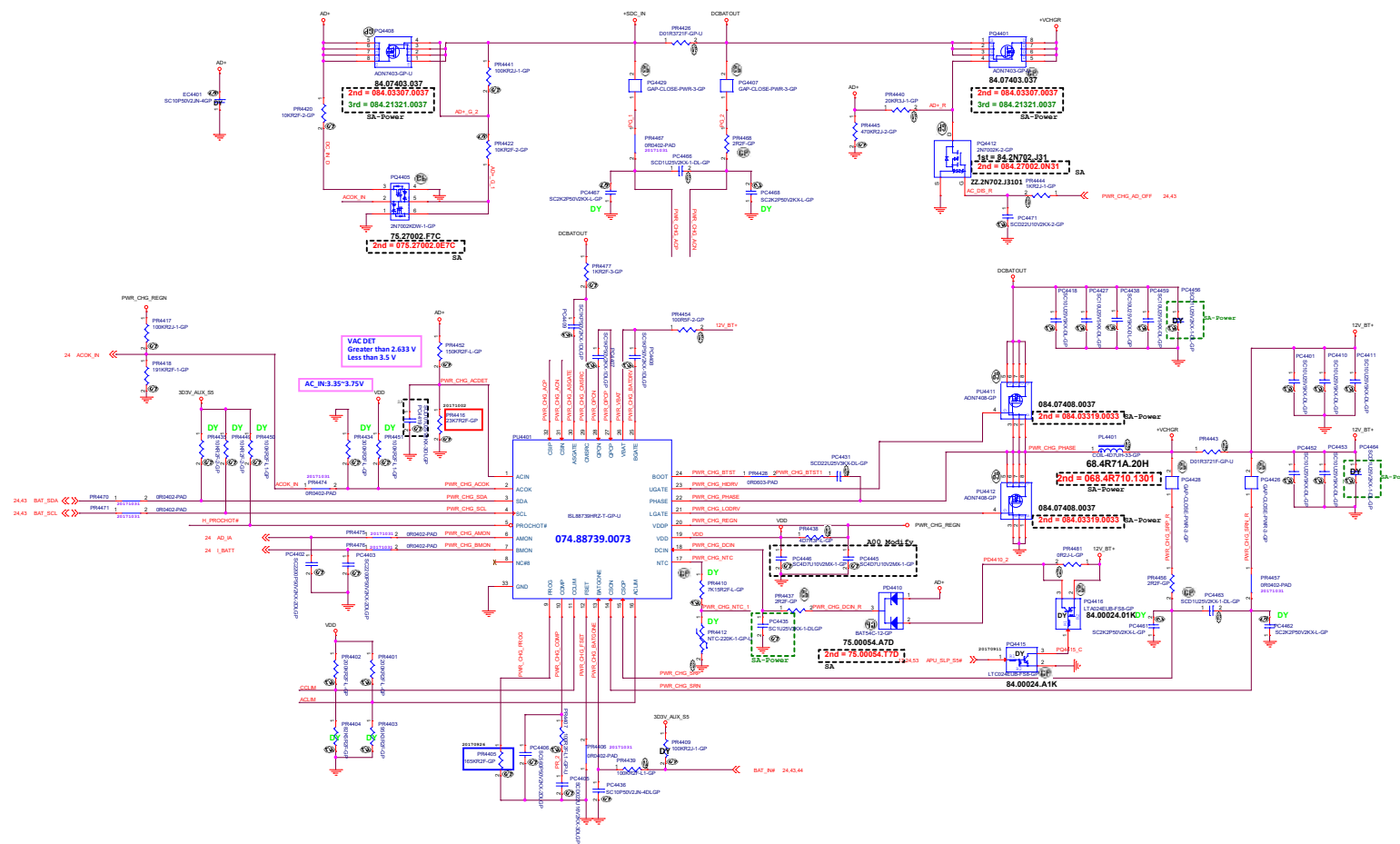
DELL **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **BATTERY CONN**

Size	Document Number	Rev
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AZ	JEAN GREY AMD	A
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Main Func = Charger



SSID = PWR.Plane.Regulator_5v3p3v

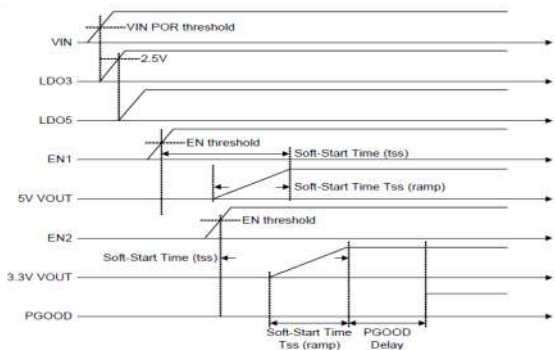
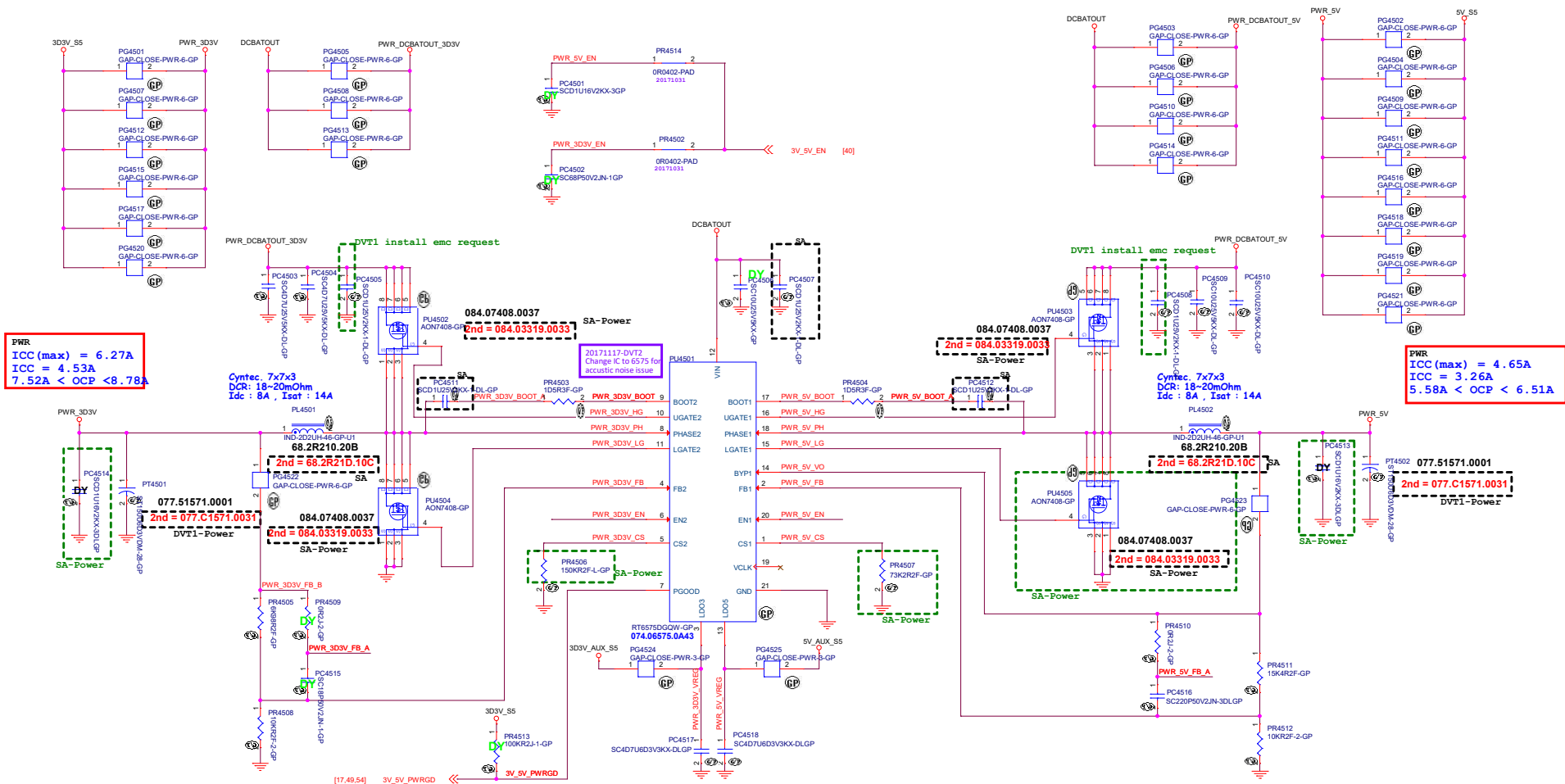
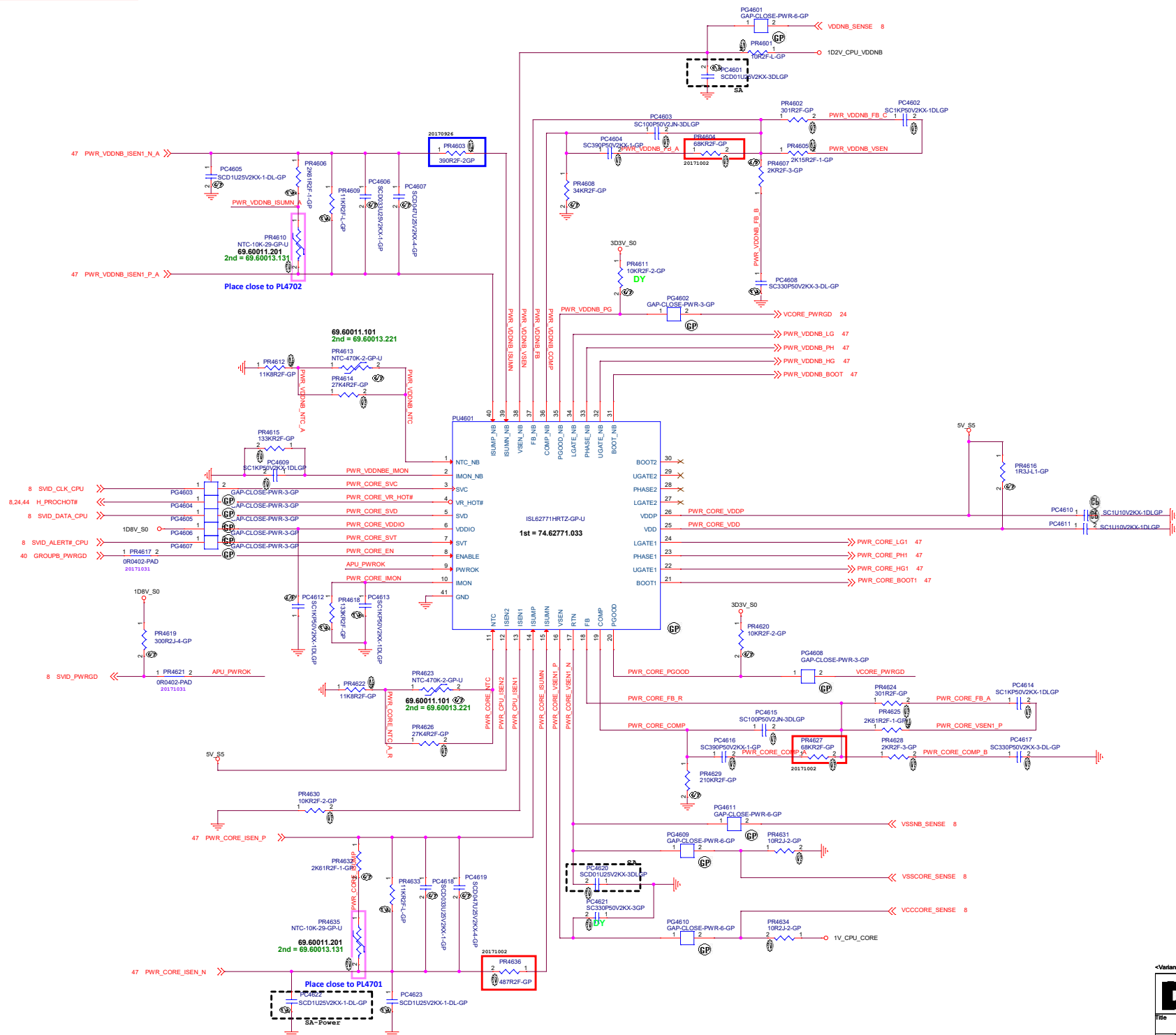


Figure 6. RT6575B Timing

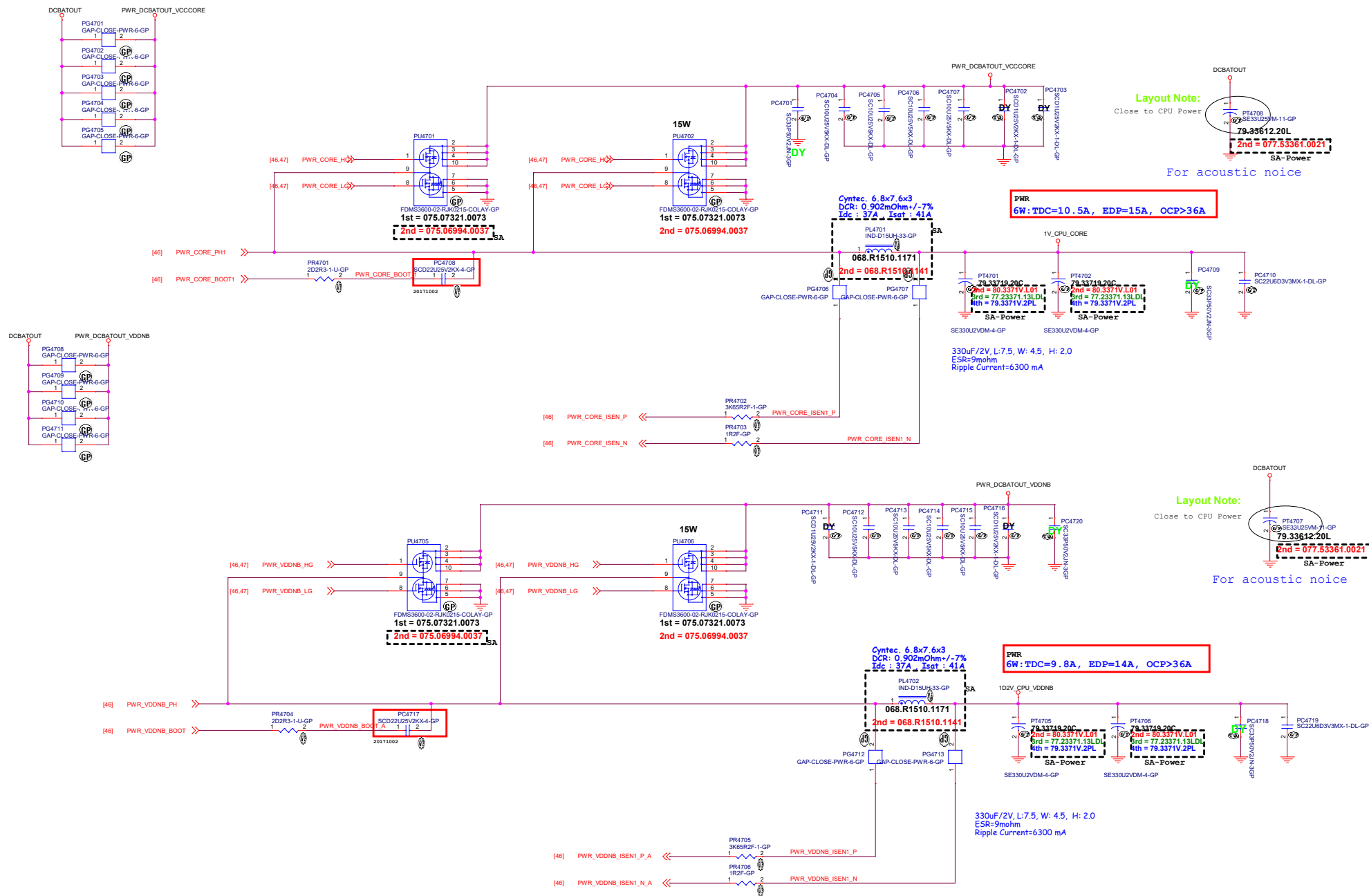
<Variant Name>



```
SSID = CPU.Regulator
```



SSID = CPU.Regulator



<Variant Name>

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Taichung Hsien 221, Taiwan, R.O.C.

ISL62771_CPUCORE(2/2)
JEAN GREY AMD
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5

4

3

2

1

D

D

C

C

B


B

A

A

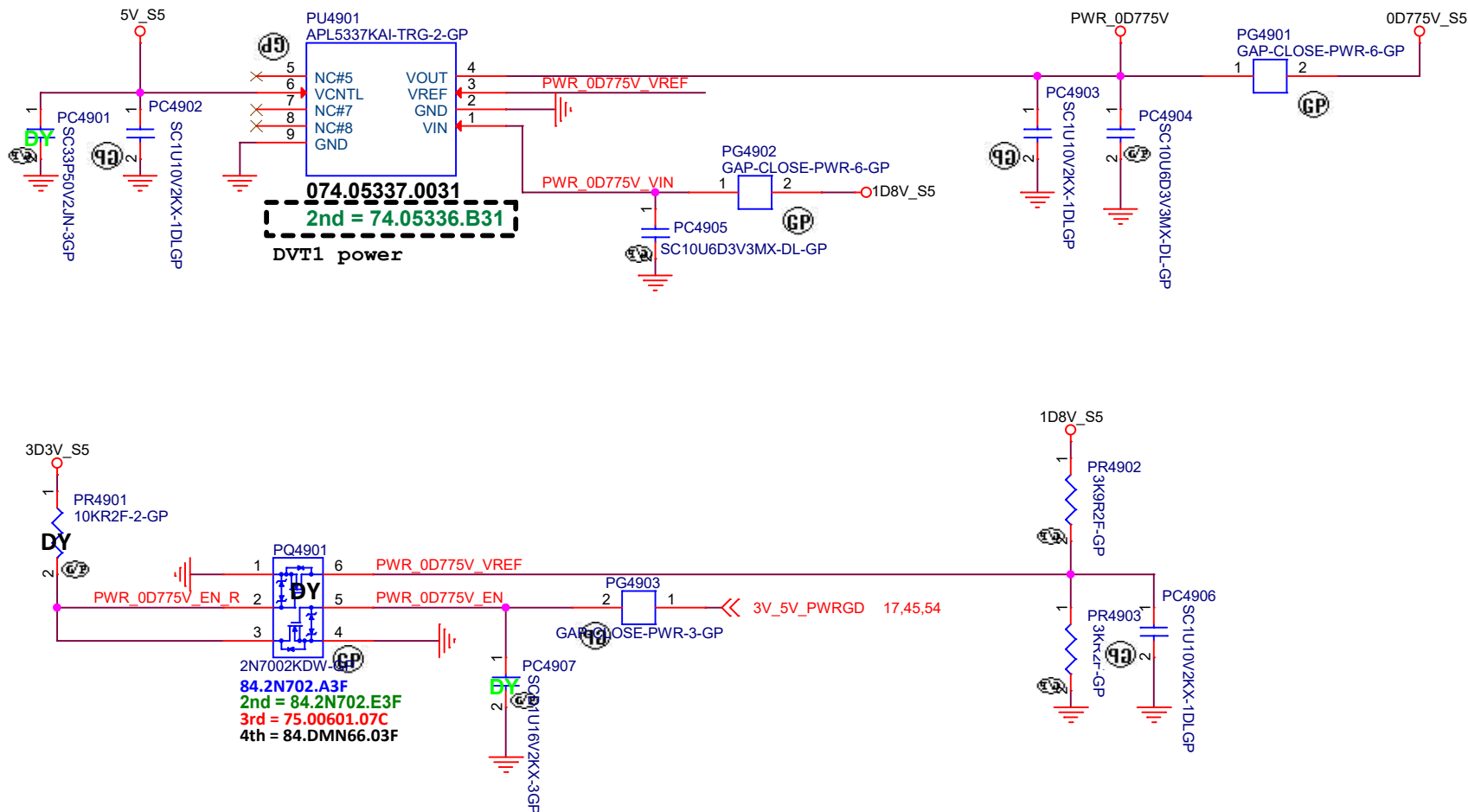
(Blanking)

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title (Reserved)					
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SSID = CPU (0D775V)

PWR
ICC = 70mA
ICC(max) = 100mA
VDDCR_FCH_S5=0.775V



<Variant Name>



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

VDDCRGFX_APL5337

Size
A4

Document Number

JEAN GREY AMD

Rev
A00


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5	4	3	2	1
D				D
C				C
B				B
A				A


(Blanking)

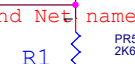
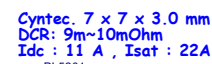
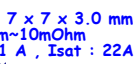
<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title (Reserved)					
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(Blanking)

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title (Reserved)					
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$$V_{out} = 0.75 * (1 + R1/R2) = 0.95V$$

Title



Document Number

JEAN GREY AMD

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SSID = VDDQ.VPP

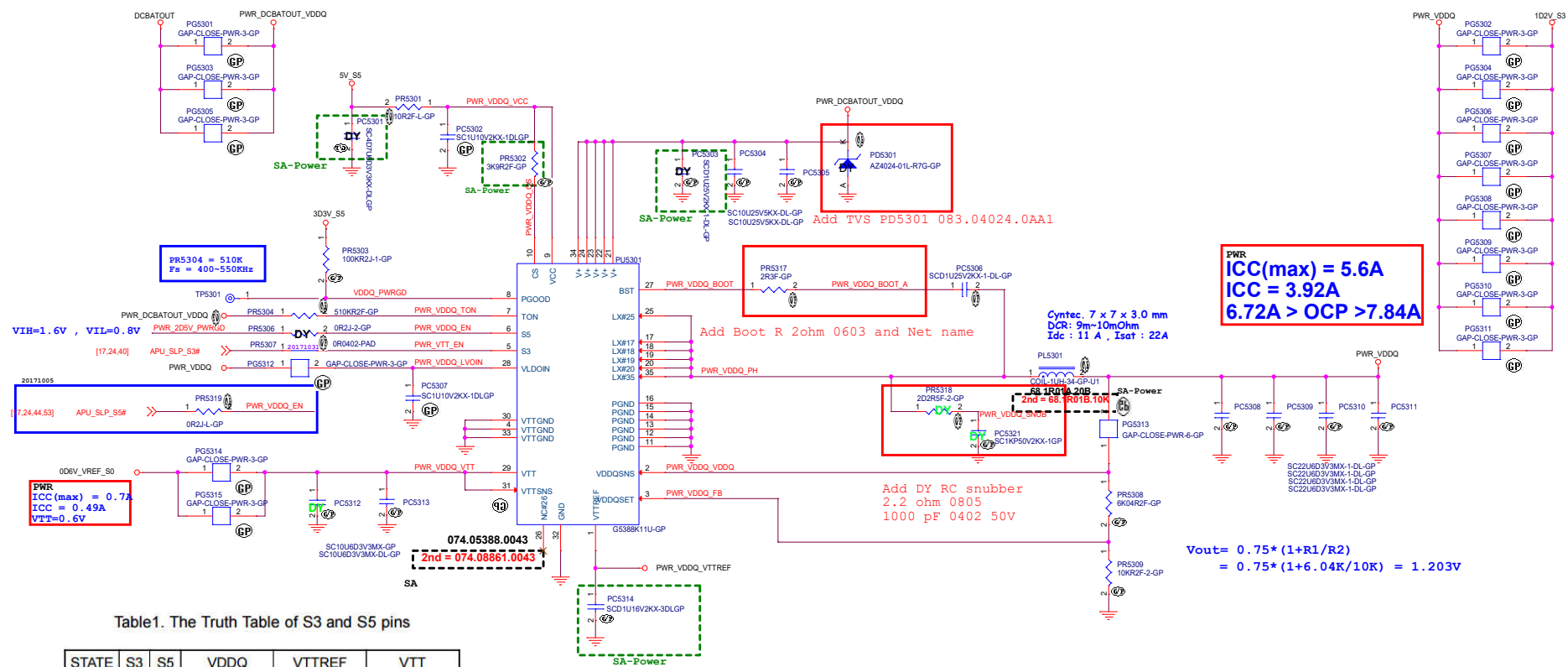
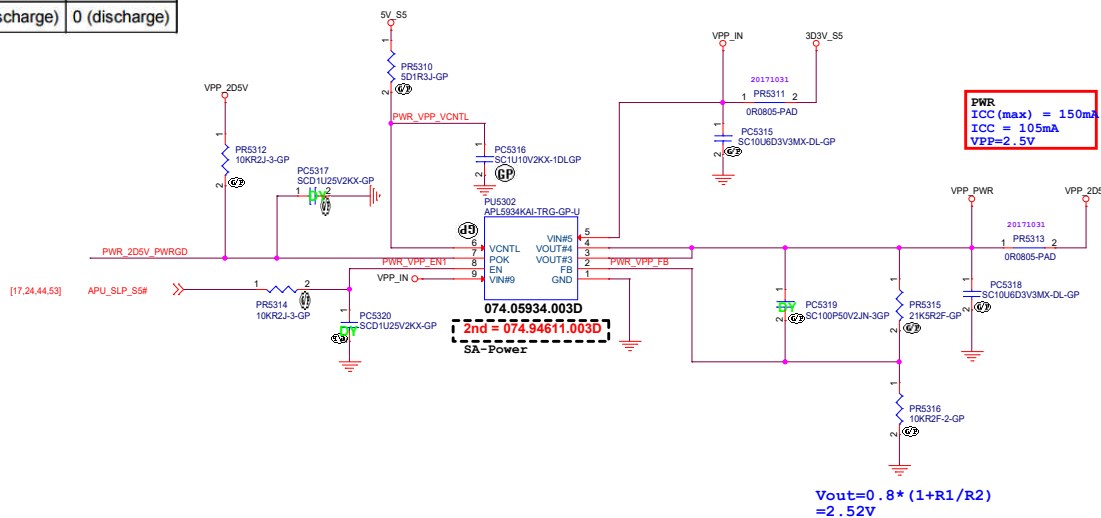


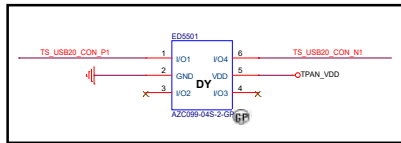
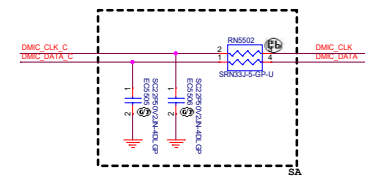
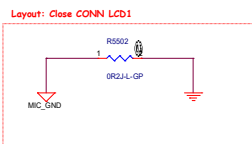
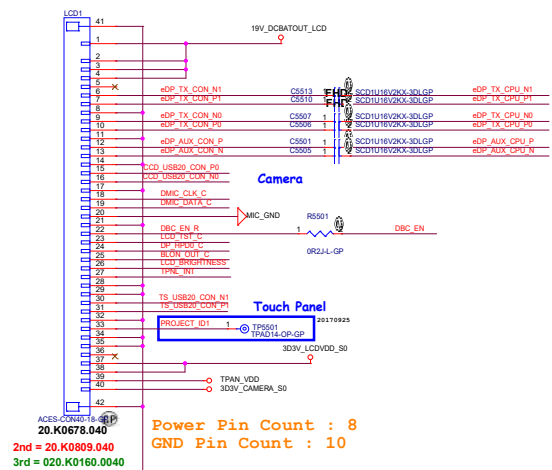
Table1. The Truth Table of S3 and S5 pins

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	H	H	1	1	1
S3	L	H	1	1	0 (high-Z)
S4/5	L	L	0 (discharge)	0 (discharge)	0 (discharge)

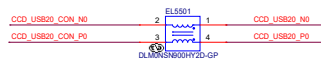


SSID = VIDEO

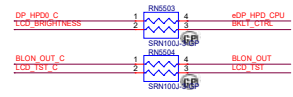
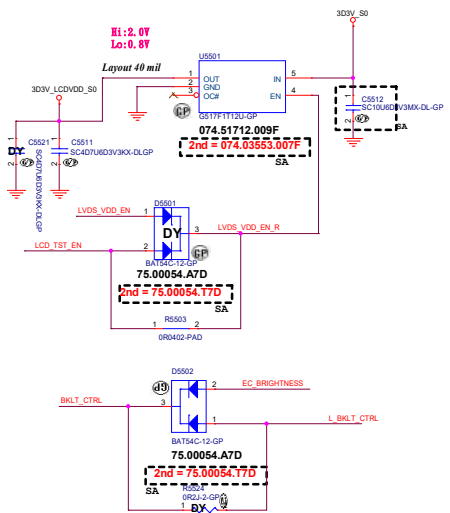
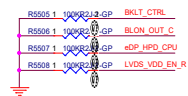
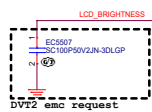
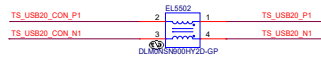
Panel Conn.



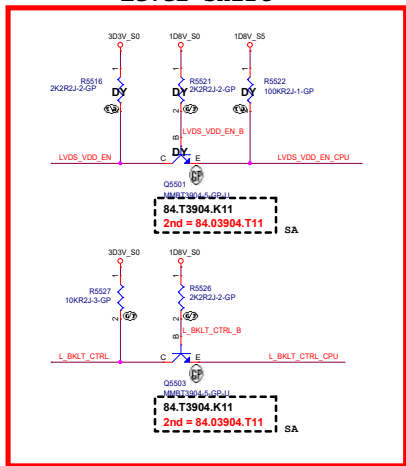
Camera



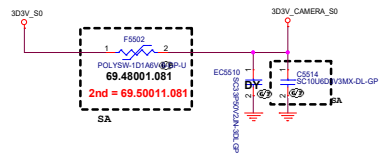
Touch Panel



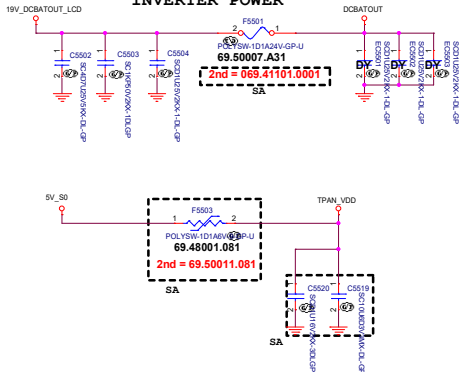
Level shift



CAMERA POWER




INVERTER POWER



<Variant Name>

Blanking

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)					
Size	Document Number				Rev
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SSID = HDMI

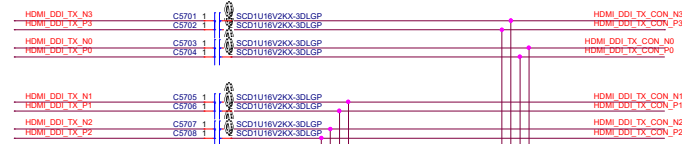
8 HDMI_DDI_TX_P0 >>>>
8 HDMI_DDI_TX_N0 >>>>
8 HDMI_DDI_TX_P1 >>>>
8 HDMI_DDI_TX_N1 >>>>
8 HDMI_DDI_TX_P2 >>>>
8 HDMI_DDI_TX_N2 >>>>
8 HDMI_DDI_TX_P3 >>>>
8 HDMI_DDI_TX_N3 >>>>

8 HDMI_SCL_CPU <<<<
8 HDMI_SDA_CPU <<<<

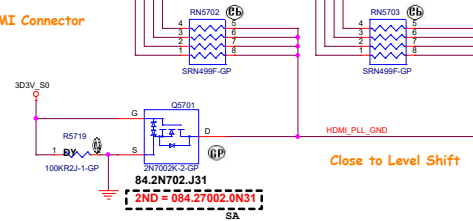
24 HDMI_IN# <<<<
8 HDMI_DET_CPU <<<<

HDMI Level Shifter & CONNECTOR

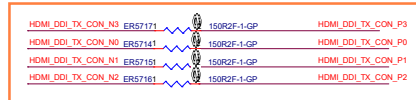
Follow Standard Net Naming rule



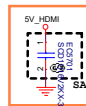
Close to HDMI Connector



Close to Level Shift

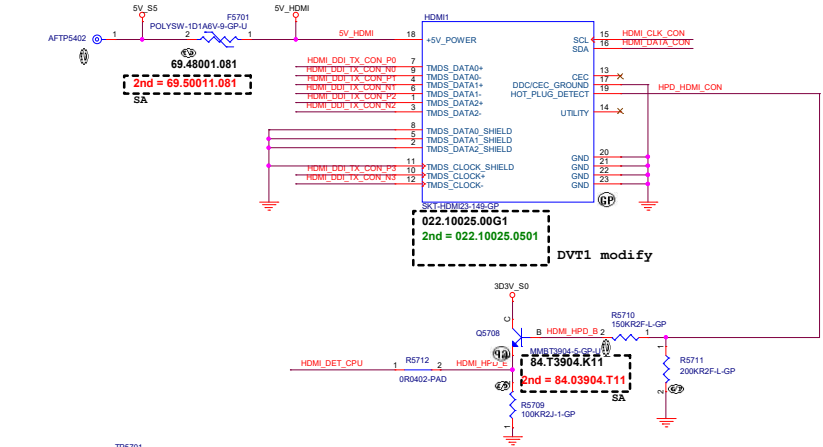


Reserve 150 ohm bridge resistance
on the HDMI trace as circle for EMI

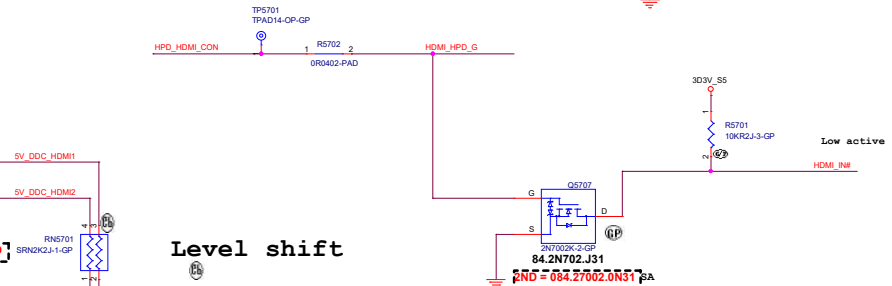


Reserve 0.1uF for ESD

HDMI CONN

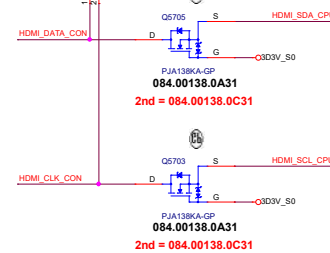


T1 modify



Low active

Level shift




2nd = 084.00138.0C31

084.00138.0A31


Blanking

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved) Display Port			
Size	Document Number JEAN GREY AMD		Rev A00
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Blanking

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved) DVI			
Size	Document Number JEAN GREY AMD		Rev A00
Date: Tuesday, April 02, 2019		Sheet 59 of	109

Blanking

<Variant Name>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

Document Number

Rev

HDD

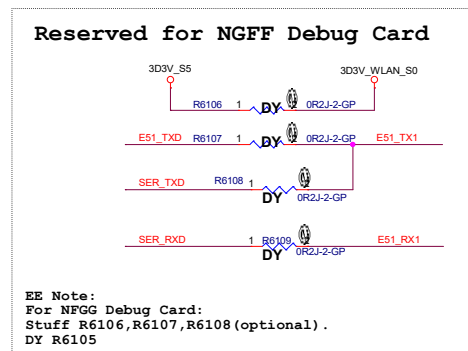
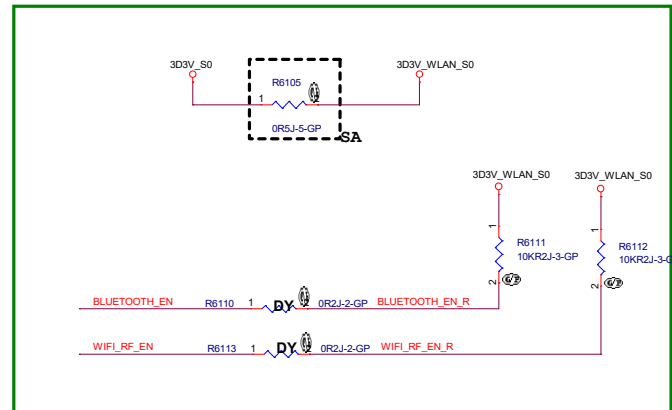
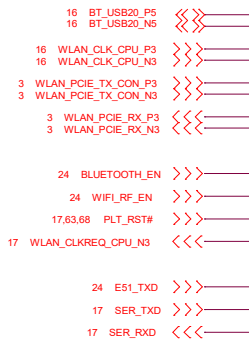
JEAN GREY AMD

A00

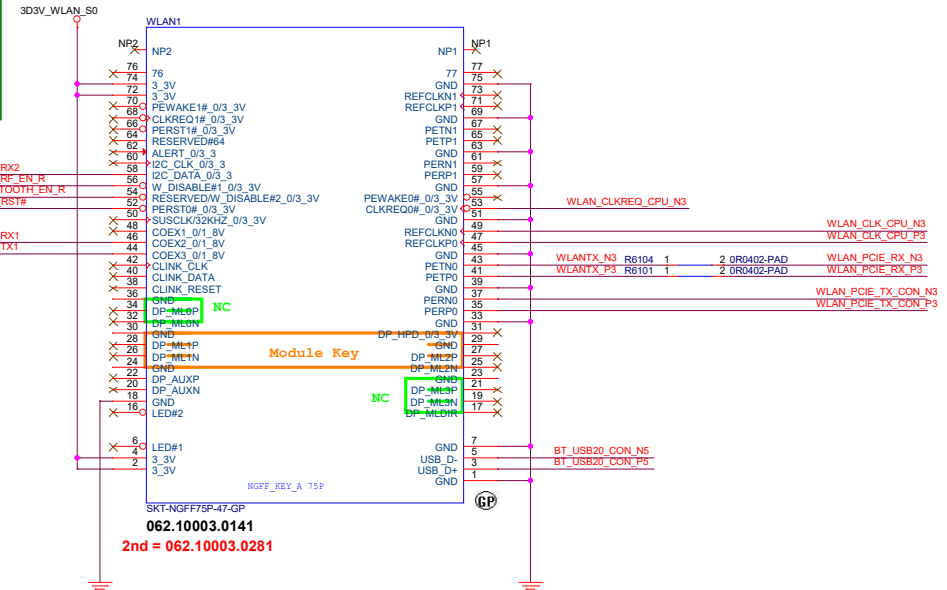
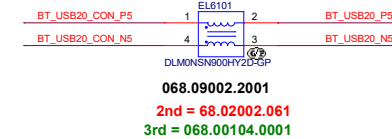
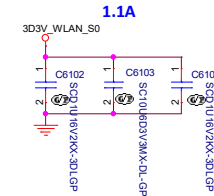
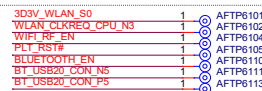
Date: Tuesday, April 02, 2019

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SSID = WLAN



EE Note:
For NFGG Debug Card:
Stuff R6106,R6107,R6108(optional).
DY R6105



<Variant Name>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **WLAN**

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	JEAN GREY AMD	A00

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Blanking

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved) WWAN			
Size	Document Number JEAN GREY AMD		Rev A00
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Timing diagram showing signals and their transitions:

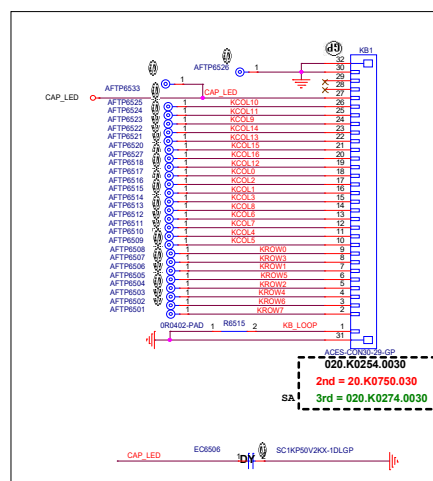
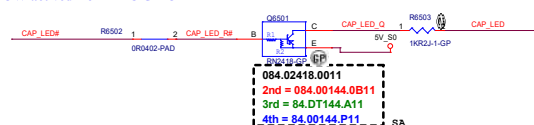
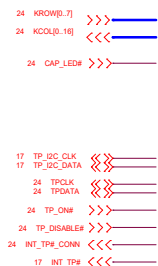
- 16 eMMC_CLK_CPU_P2
- 16 eMMC_CLK_CPU_N2
- 3 eMMC_PCIE_TX_C_P2
- 3 eMMC_PCIE_TX_C_N2
- 3 eMMC_PCIE_RX_P2
- 3 eMMC_PCIE_RX_N2
- 7 eMMC_CLKREQ_CPU_N2
- 17.61.68 PLT_RST#



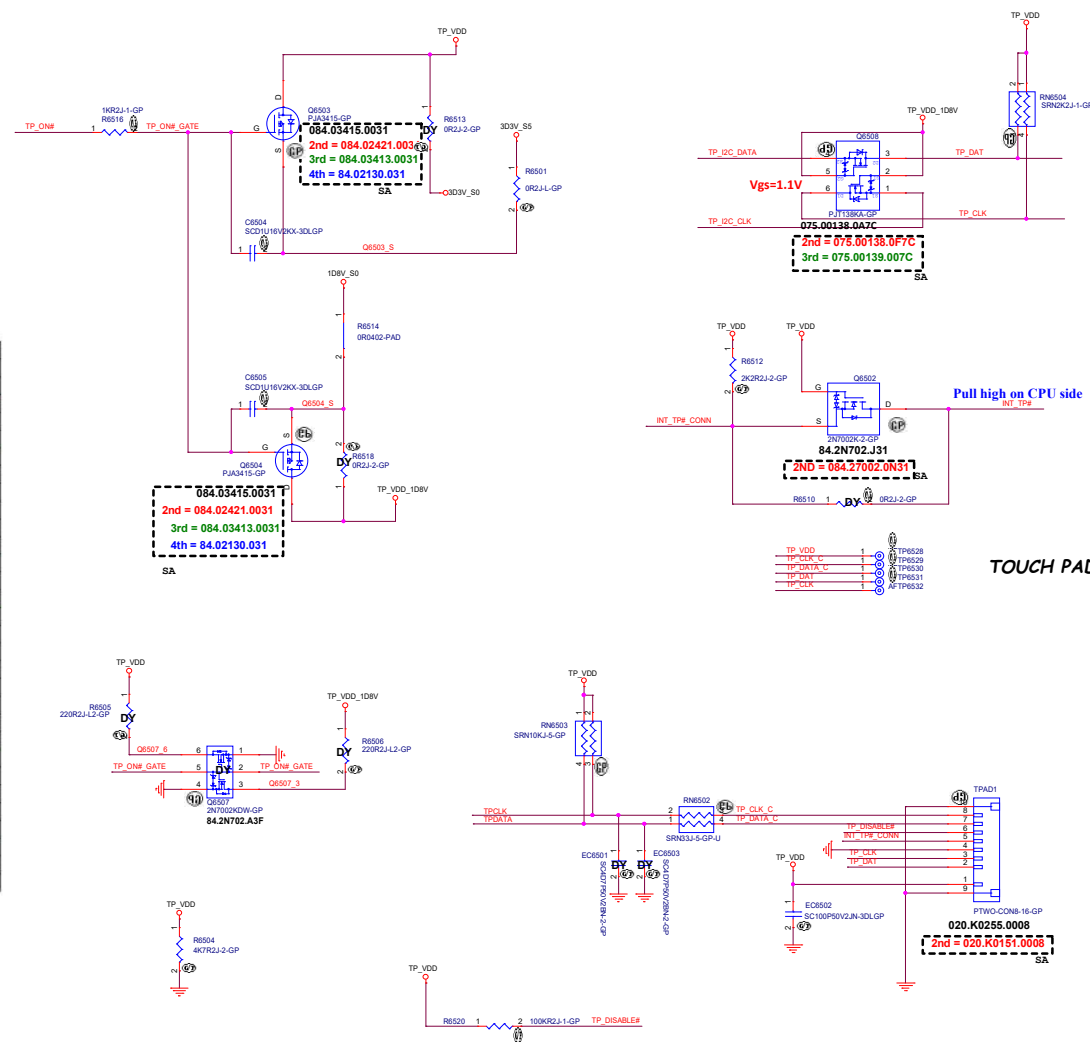
Blanking

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title LED / PWRBTN			
Size A4	Document Number JEAN GREY AMD		Rev A00
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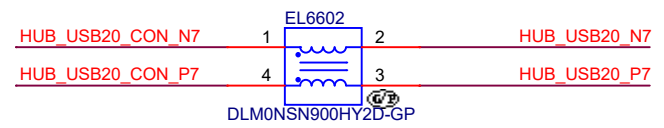
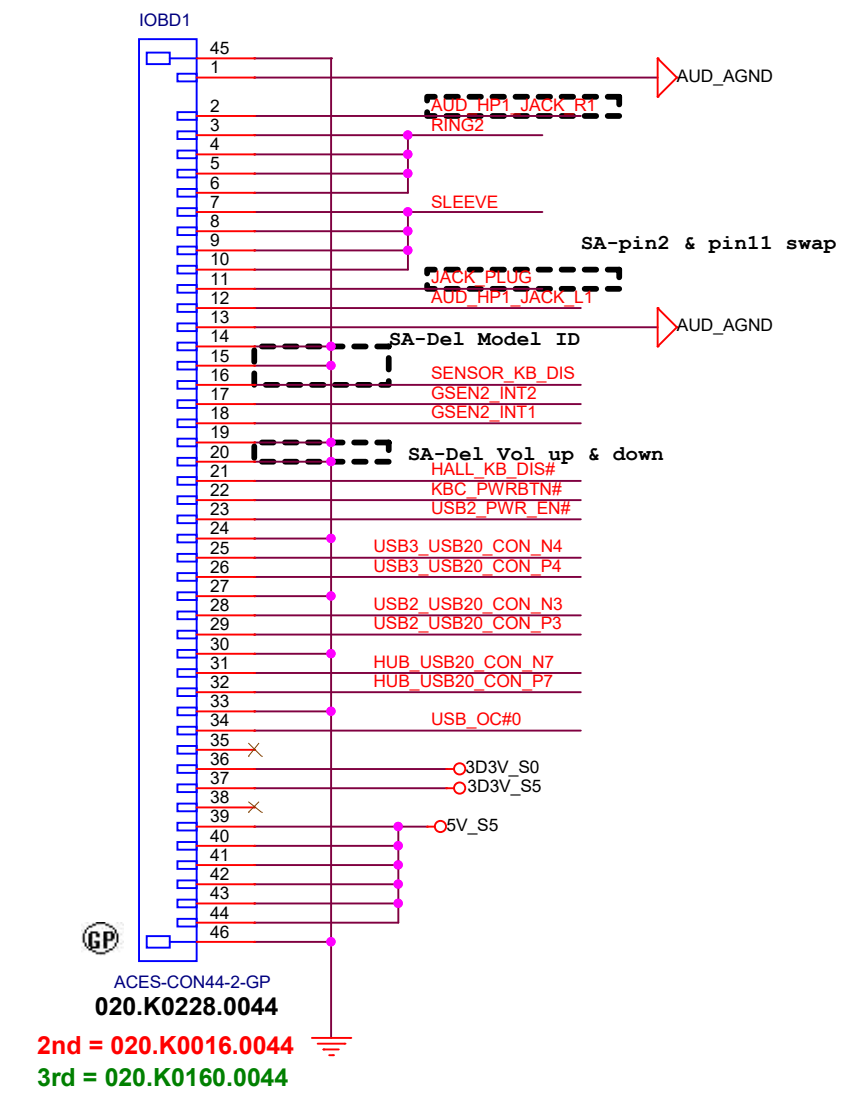


PIN	SIGNAL
1	Diag_Loop-GPIO_1 (TPC)
2	KSI [1] : R80 S8
3	KSI [4] : R80 S7
4	KSI [4] : R80 S5
5	KSI [23] : R80 S3
6	KSI [15] : R80 S6
7	KSI [11] : R80 S2
8	KSI [13] : R80 S4
9	KSI [0] : R80 S1
10	KSD [5] : R80 D6
11	KSD [4] : R80 D5
12	KSD [7] : R80 D8
13	KSD [6] : R80 D7
14	KSD [8] : R80 D9
15	KSD [13] : R80 D4
16	KSD [11] : R80 D2
17	KSD [2] : R80 D3
18	KSD [0] : R80 D1
19	KSD [12] : R80 D13
20	KSD [16] : R80 D17
21	KSD [15] : R80 D16
22	KSD [13] : R80 D14
23	KSD [14] : R80 D15
24	KSD [19] : R80 D19
25	KSD [11] : R80 D12
26	KSD [10] : R80 D11
27	Copack LED
28	N/C
29	N/C
30	GND



SSID = IO Connector

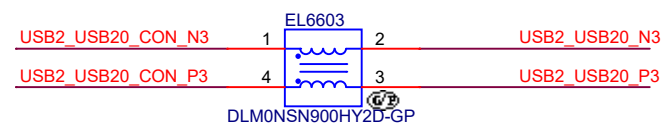
29	JACK_PLUG	<<<	---
29	RING2	<<<	---
29	SLEEVE	<<<	---
29	AUD_HP1_JACK_R1	>>>	---
29	AUD_HP1_JACK_L1	>>>	---
24	SENSOR_KB_DIS	<<<	---
69	GSEN2_INT2	>>>	---
69	GSEN2_INT1	>>>	---
24	HALL_KB_DIS#	<<<	---
24	KBC_PWRBTN#	<<<	---
24	USB2_PWR_EN#	>>>	---
17	USB_OC#0	<<<	---
16	HUB_USB20_P7	>>>	---
16	HUB_USB20_N7	>>>	---
16	USB2_USB20_P3	>>>	---
16	USB2_USB20_N3	>>>	---
16	USB3_USB20_N4	>>>	---
16	USB3_USB20_P4	>>>	---



068.09002.2001

2nd = 68.02002.061

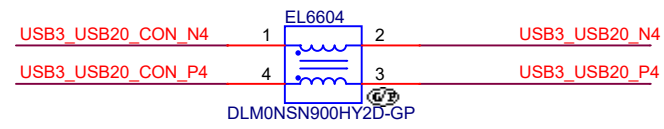
3rd = 068.00104.0001



068.09002.2001

2nd = 68.02002.061

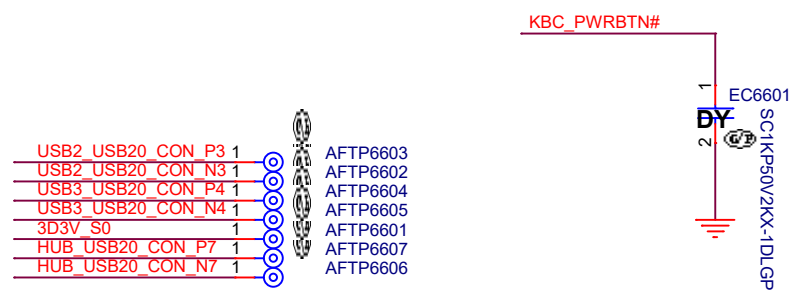
3rd = 068.00104.0001




068.09002.2001

2nd = 68.02002.061

3rd = 068.00104.0001



<Variant Name>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

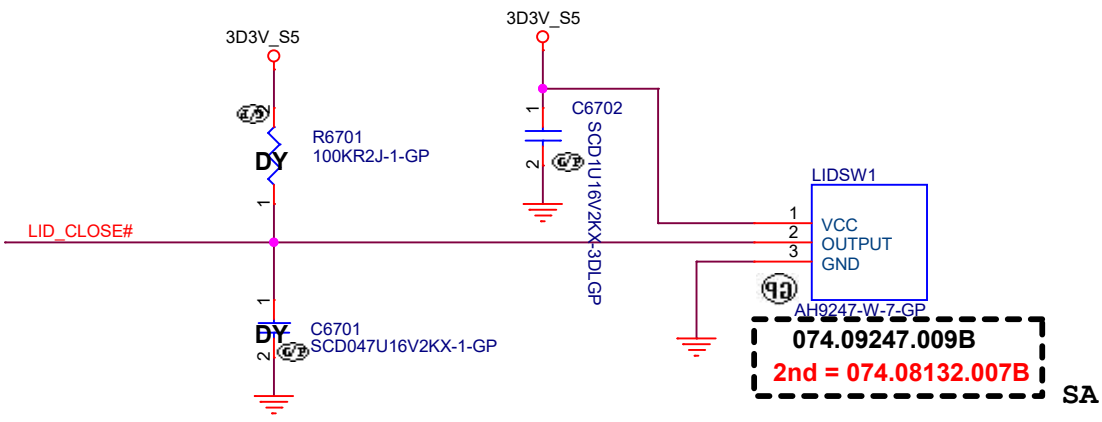
Title **IO Board CONN**

Size A4	Document Number JEAN GREY AMD	Rev A00
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SSID = Hall Sensor

24 LID_CLOSE# <<<—



<Variant Name>

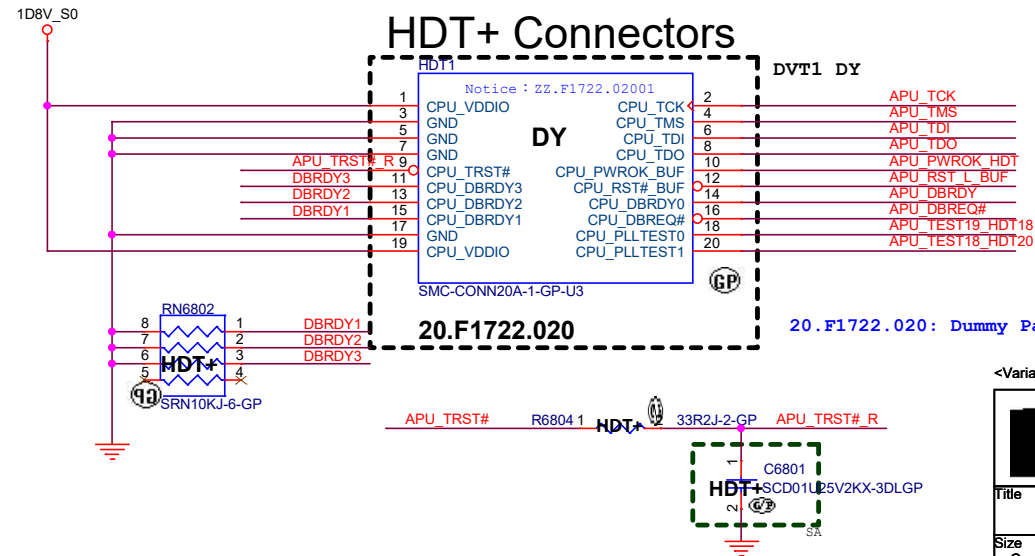
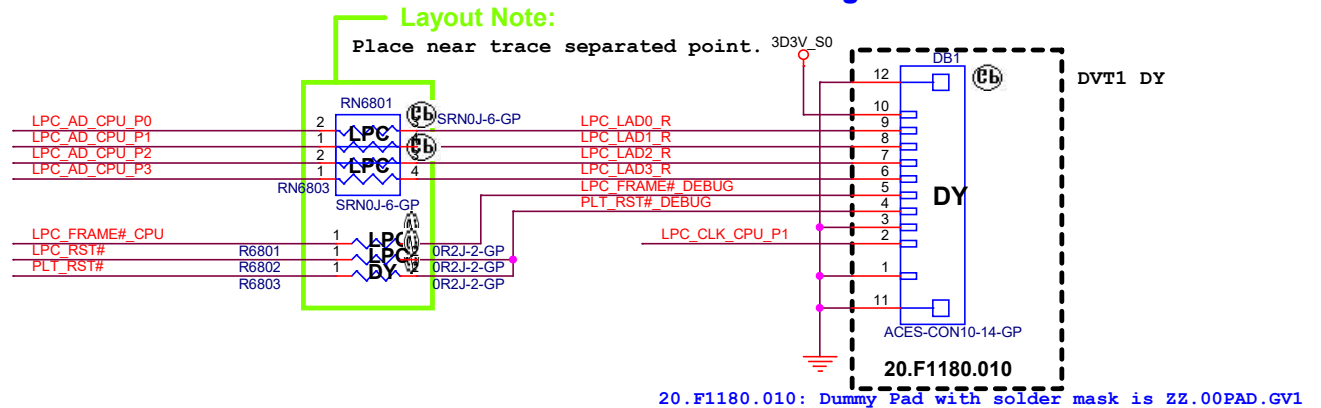
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Hall Sensor			
Size A4	Document Number JEAN GREY AMD		Rev A00
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SSID = DEBUG PORT

16,24 LPC_AD_CPU_P0 <<>>—
16,24 LPC_AD_CPU_P1 <<>>—
16,24 LPC_AD_CPU_P2 <<>>—
16,24 LPC_AD_CPU_P3 <<>>—
16,20,24 LPC_FRAME#_CPU <<>>—

16,24 LPC_RST# >>>—
17,61,63 PLT_RST# >>>—
16 LPC_CLK_CPU_P1 >>>—

8 APU_TRST# <<>>—
8 APU_TCK <<>>—
8 APU_TMS <<>>—
8 APU_TDI <<>>—
8 APU_TDO <<>>—
8 APU_PWROK_HDT <<>>—
8 APU_RST_L_BUF <<>>—
8 APU_DBRDY <<>>—
8 APU_DBREQ# <<>>—
8 APU_TEST19_HDT18 <<>>—
8 APU_TEST18_HDT20 <<>>—

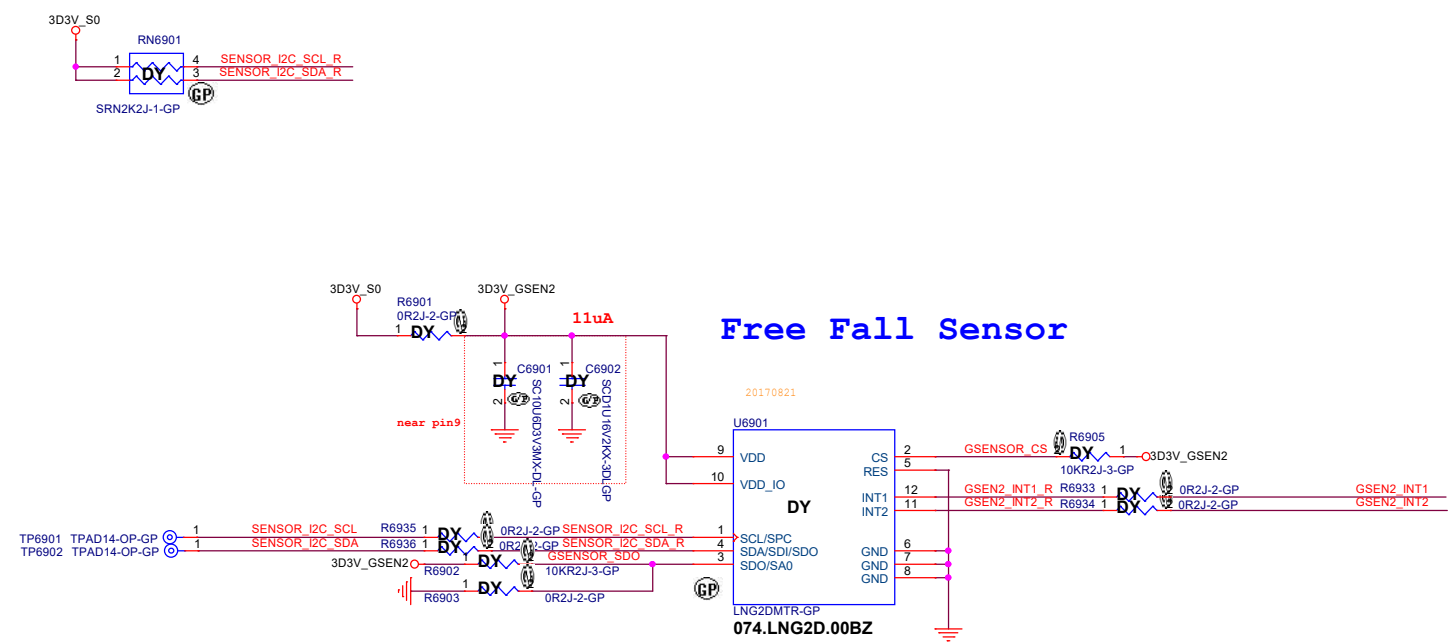


<Variant Name>

DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Debug connector			
Size Custom	Document Number JEAN GREY AMD		Rev A00
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SSID = Sensor

24 GSEN2_INT1 <<<—
24 GSEN2_INT2 <<<—




Blanking

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Free Fall Sensor			
Size	Document Number		Rev
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Blanking

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title (Reserved)Thunderbolt (1/5)		
Size A4	Document Number JEAN GREY AMD	Rev A00
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Blanking

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)Thunderbolt (2/5)					
Size		Document Number			Rev
A4		JEAN GREY AMD			A00
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Blanking

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)Thunderbolt (3/5)					
Size		Document Number			Rev
A4		JEAN GREY AMD			A00
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Blanking

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title (Reserved)Thunderbolt (4/5)		
Size A4	Document Number JEAN GREY AMD	Rev A00
Date: Tuesday, April 02, 2019		Sheet 74 of 109


Blanking

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title (Reserved)Thunderbolt (5/5)		
Size A4	Document Number JEAN GREY AMD	Rev A00
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Blanking

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)GPU (1/5) PEG					
Size		Document Number			Rev
A4		JEAN GREY AMD			A00
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Blanking

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)GPU (2/5) DIGITAL					
Size		Document Number			Rev
A4		JEAN GREY AMD			A00
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Blanking

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)GPU (3/5) VRAM					
Size		Document Number			Rev
A4		JEAN GREY AMD			A00
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Blanking

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title (Reserved)GPU (4/5) GPIO		
Size A4	Document Number JEAN GREY AMD	Rev A00
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Blanking

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)GPU (5/5) PWR/GND					
Size		Document Number			Rev
A4		JEAN GREY AMD			A00
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Blanking

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)VRAM1,2 (1/4)					
Size		Document Number			Rev
A4		JEAN GREY AMD			A00
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Blanking

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)VRAM3,4 (2/4)					
Size		Document Number			Rev
A4		JEAN GREY AMD			A00
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Blanking

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)VRAM5,6 (3/4)					
Size		Document Number			Rev
A4		JEAN GREY AMD			A00
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Blanking

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserved)VRAM7,8 (4/4)					
Size		Document Number			Rev
A4		JEAN GREY AMD			A00
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Blanking

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title (Reserved)VGA_CORE		
Size A4	Document Number JEAN GREY AMD	Rev A00
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Blanking

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title (Reserved)DISCRETE VGAPOWER					
Size	Document Number JEAN GREY AMD				Rev A00
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Blanking

<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number JEAN GREY AMD		Rev A00
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Blanking

<Variant Name>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title (Reserved)					
Size A4		Document Number JEAN GREY AMD			Rev A00
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Main Func = UnusedParts

34.43E24.001

SPRING-13-GP-U
SPR1



34.4Y806.001

SPR2
SPRING-63-GP



34.34S02.002

SPRING-98-GP
SPR3



34.34S02.002

SPRING-98-GP
SPR4



34.34S02.002

SPRING-98-GP
SPR5



34.34S02.002

SPRING-98-GP
SPR6



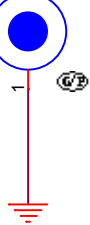
ZZ.PAD01.041

H1
HOLE354R237-GP



ZZ.00PAD.YF1

H10
HOLE276R182-GP



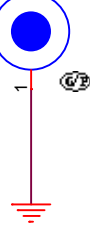
ZZ.00PAD.YF1

H11
HOLE276R182-GP



ZZ.00PAD.YF1

H12
HOLE276R182-GP



ZZ.00PAD.YF1

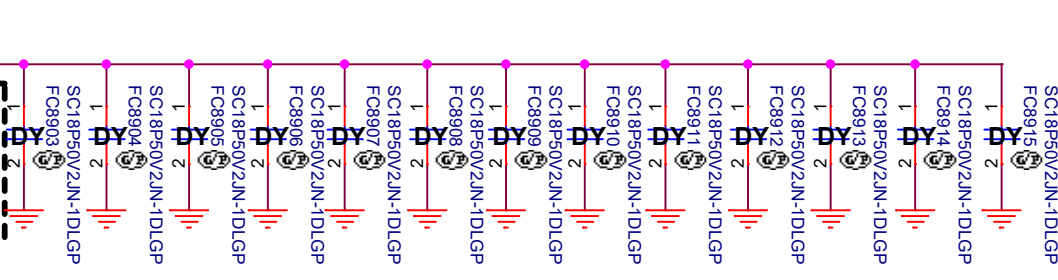
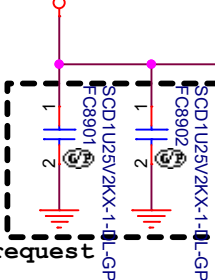
H13
HOLE276R182-GP



DVT1 modify

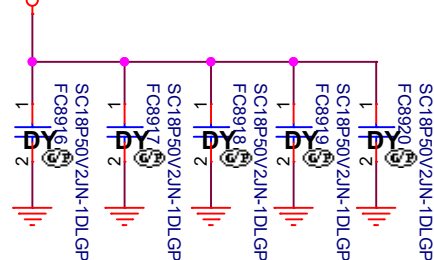
Main Func = EMI & RF Capacitors

DCBATOUT

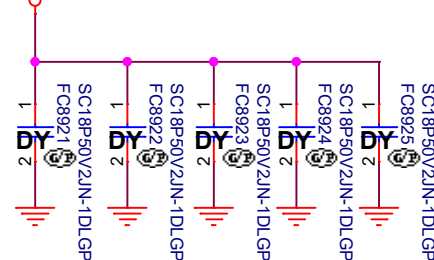


DVT1 emc request

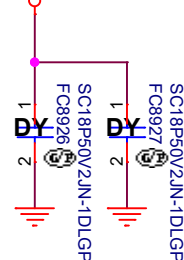
3D3V_S0



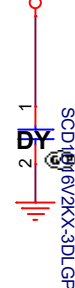
5V_S0



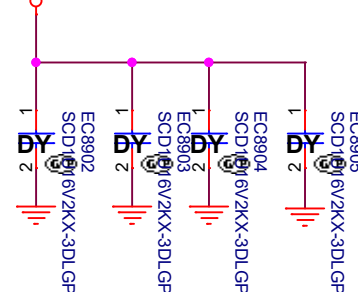
0D95V_S0



5V_S5



3D3V_S0



<Variant Name>



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UNUSED PARTS/EMI Capacitors

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Title (Reserved)NFC Connector					
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<Variant Name>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
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Title
(Reserved)Express Card

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Title					
(Reserved)Smart Card Socket					
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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title (Reserved)SW GFX eDP					
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title (Reserved)Bottom Docking		
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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
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Title			
CPU_XDP			
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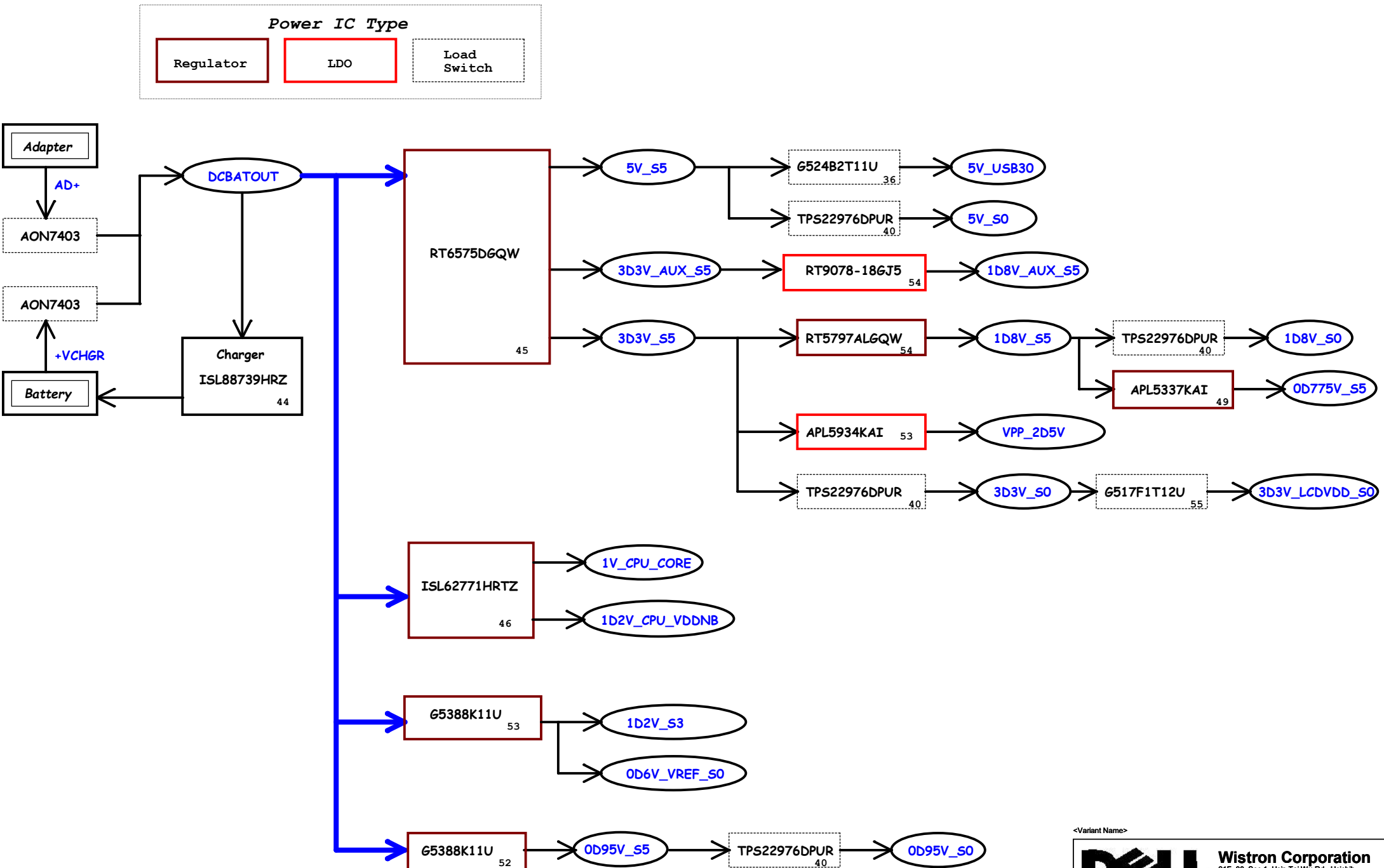
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002_Block Diagram	038_(Reserved)	074_(Reserved)
003_CPU (PCIE)	039_DISCHARGE	075_(Reserved)
004_(Reserved)	040_Power Plane Enable&Sequence	076_(Reserved) GPU(1/5) PEG
005_CPU (DDR)	041_(Reserved)	077_(Reserved) GPU (2/5) DIGITALOUT
006_(Reserved)	042_(Reserved)	078_(Reserved) GPU (3/5) VRAM I/F
007_CPU(VCC CORE)	043_DCIN JACK & BATT Conn	079_(Reserved) GPU (4/5) GPIO/STRAP
008_CPU (DISPLAY/SVI2/JTAG/TES)	044_CHARGER ISL88739	080_(Reserved) GPU (5/5) PWR/GND
009_CPU (VSS)	045_TPS51225RUKR 5V/3D3V	081_(Reserved) VRAM1,2 (1/2)
010_CPU (Power CAP1)	046_ISL62771 CPUCORE(1/2)	082_(Reserved) VRAM3,4 (2/2)
011_(Reserved)	047_ISL62771 CPUCORE(2/2)	083_(Reserved)
012_DDR4-SODIMM1	048_(Reserved)	084_(Reserved)
013_(Reserved) DDR4-SODIMM2	049_VDDCRGFX APL5337	085_(Reserved) GPU CORE ISL62771HRTZ
014_(Reserved)	050_(Reserved)	086_(Reserved) DISCRETE VGAPOWER
015_(Reserved)	051_(Reserved)	087_(Reserved)
016_CPU (CLK/SATA/USB/SPI/LPC)	052_APW8861 0D95V	088_(Reserved)
017_CPU (ACPI/SD/AZ/GPIO/RTC)	053_VDDQ&VTT&VPP APW8861	089_UNUSED PARTS/EMI Capacitors
018_(Reserved)	054_DC2DC 1D8V/1D5V	090_(Reserved)
019_(Reserved)	055_LCD/Inverter CONN	091_(Reserved)
020_CPU Strappings	056_(Reserved) VGA	092_(Reserved)
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024_KBC Nuvoton NPCE385	060_SATA IF HDD/ODD	096_(Reserved)
025_Flash(KBC+PCH)/RTC	061_NGFF WLAN CONN	097_(Reserved)
026_THERMAL NCT7718W/Fan	062_(Reserved)	098_(Reserved)
027_Audio Codec ALC3204	063_(Reserved)	099_(Reserved)
028_(Reserved)	064_LED Board&Power Button	100_Table of Content
029_Speaker/HPMIC	065_Key Board&Touch Pad	101_Power Block Diagram
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031_(Reserved) LAN RTL8111/RTL810	067_(Reserved)	103_Power Down Sequence Diagram
032_(Reserved) RJ45&Transformer	068_Debug connector	104_SMBUS BLOCK DIAGRAM
033_Card Reader	069_(Reserved)	105_THERMAL/AUDIO BLOCK DIAGRAM
034_(Reserved) USB2.0 CONN	070_(Reserved) Hall Sensor	106_CLK / USB Block Diagram
035_USB3.0 CONN	071_(Reserved)	
036_USB Power SW	072_(Reserved)	

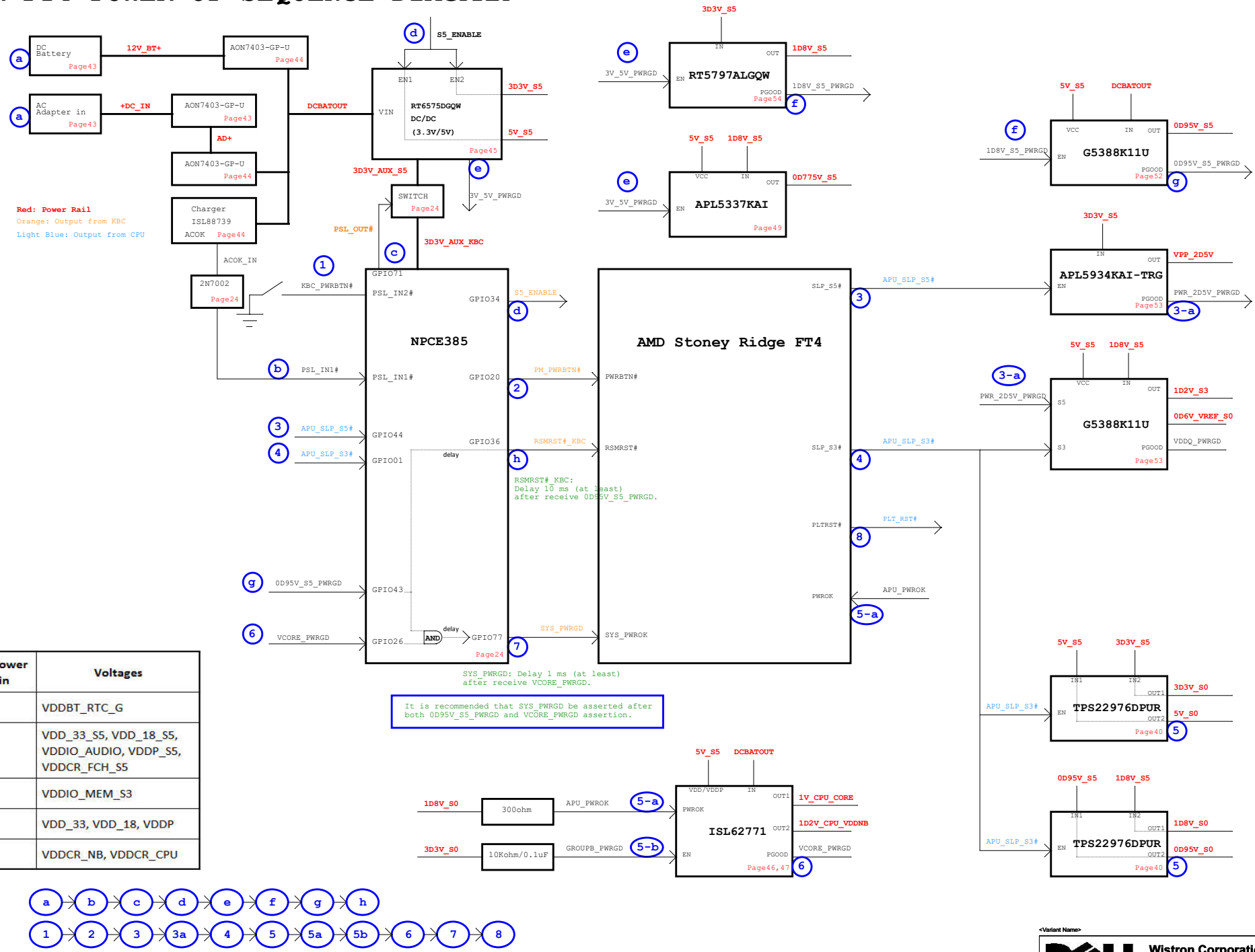
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Jean grey STR-FT4 POWER UP SEQUENCE DIAGRAM



Group	System Power Domain	Voltages
Group A	G3	VDDBT_RTC_G
Group B	S5	VDD_33_S5, VDD_18_S5, VDDIO_AUDIO, VDDP_S5, VDDCR_FCH_S5
Group C	S3	VDDIO_MEM_S3
	S0	VDD_33, VDD_18, VDDP
Group D	S0	VDDCR_NB, VDDCR_CPU

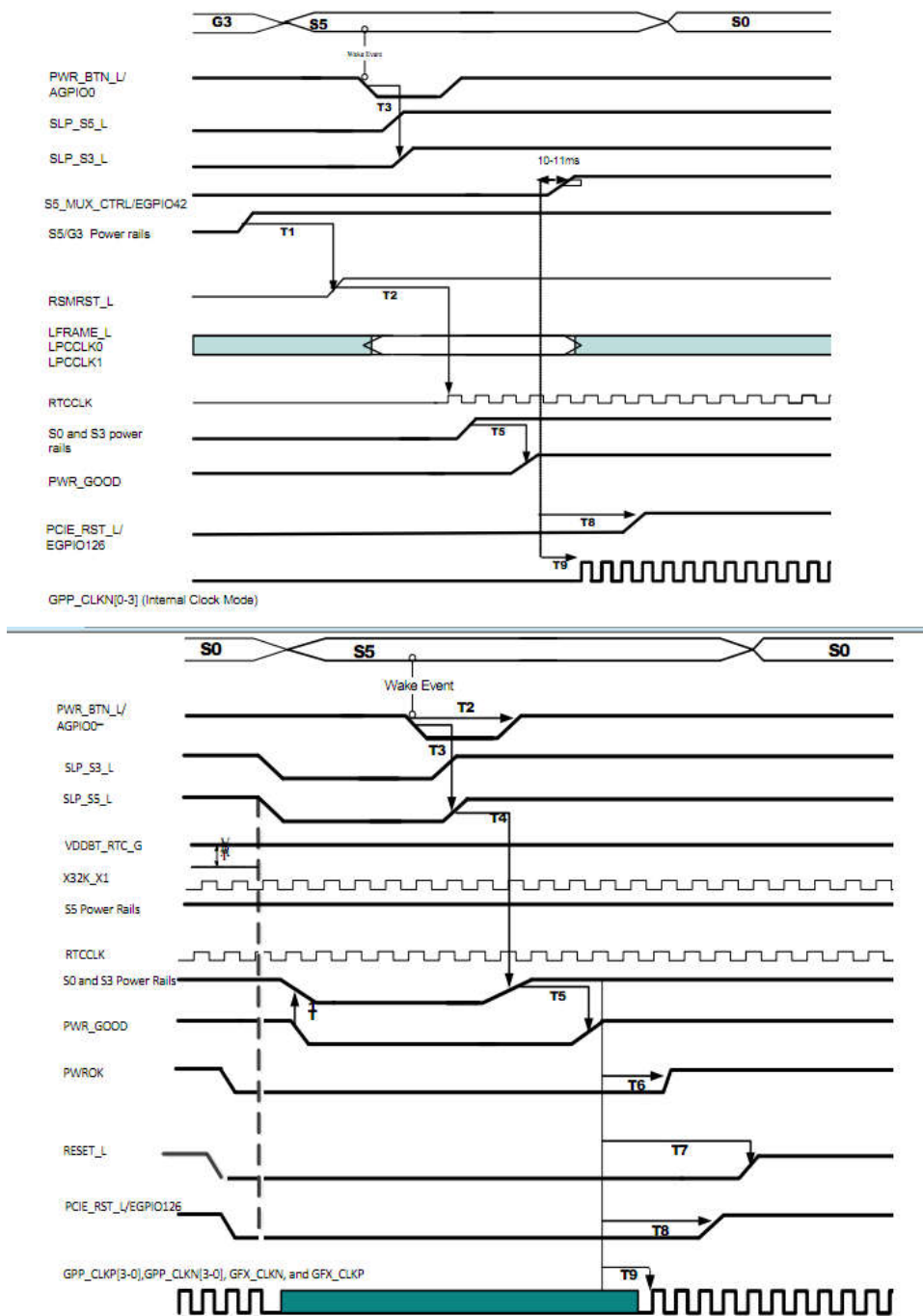


Figure 8. S0->S5->S0 Power Sequence Timing Diagram

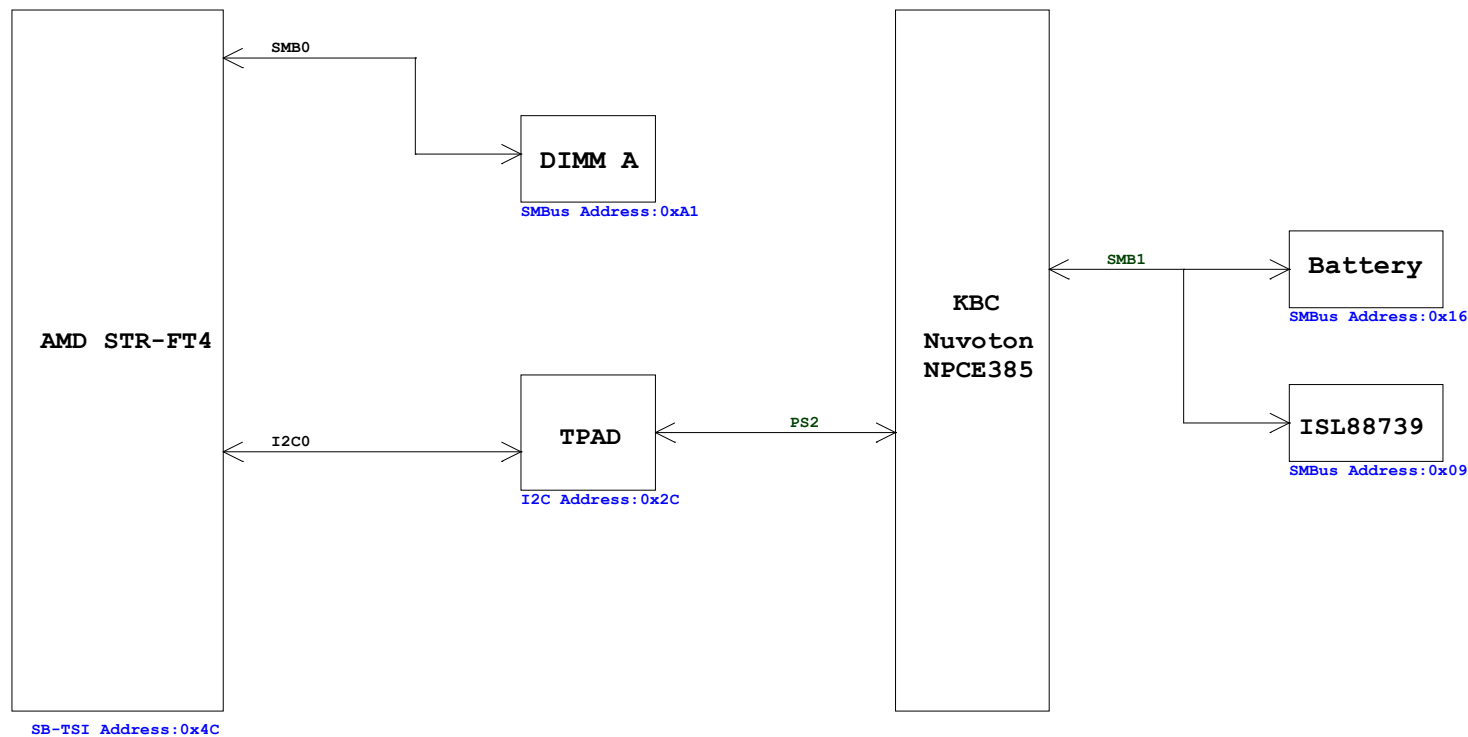
Table 58. G3->S5->S0 Reset Sequencing Timing Parameters without coin cell battery

Parameter	Max	Typical	Min	Description
T1			10ms	From S5 power rails to RSMRST_L. *This could take up to 5 seconds if power has been removed from VDDBT_RTC_G.
T2	16.5ms		15.5ms	From RSMRST_L to RTCCLK. *This timing applies after RTCCLK on the X1 input is stable and greater than 28KHz.
T3	138us		106us	From PWR_BTN_L/AGPIO0(falling) to SLP_S3_L(rising) and SLP_S5_L(rising). *This timing applies after RTCCLK on the X1 input is stable and greater than 28KHz.
T5			1ms	From power rails stable to PWR_GOOD (rising).
T8	16ms		15ms	From PWR_GOOD (rising) to PCIE_RST_L/EGPIO126 (rising). *This timing applies after RTCCLK on the X1 input is stable and greater than 28KHz.
T9	20ms		12ms	From PWR_GOOD (rising) to clock (GFX_CLKP/N, GPP_CLKP [0-3], and GPP_CLKN[0-3]) stable.

Table 59. G3->S5->S0 Reset Sequencing Timing Parameter with coin cell battery

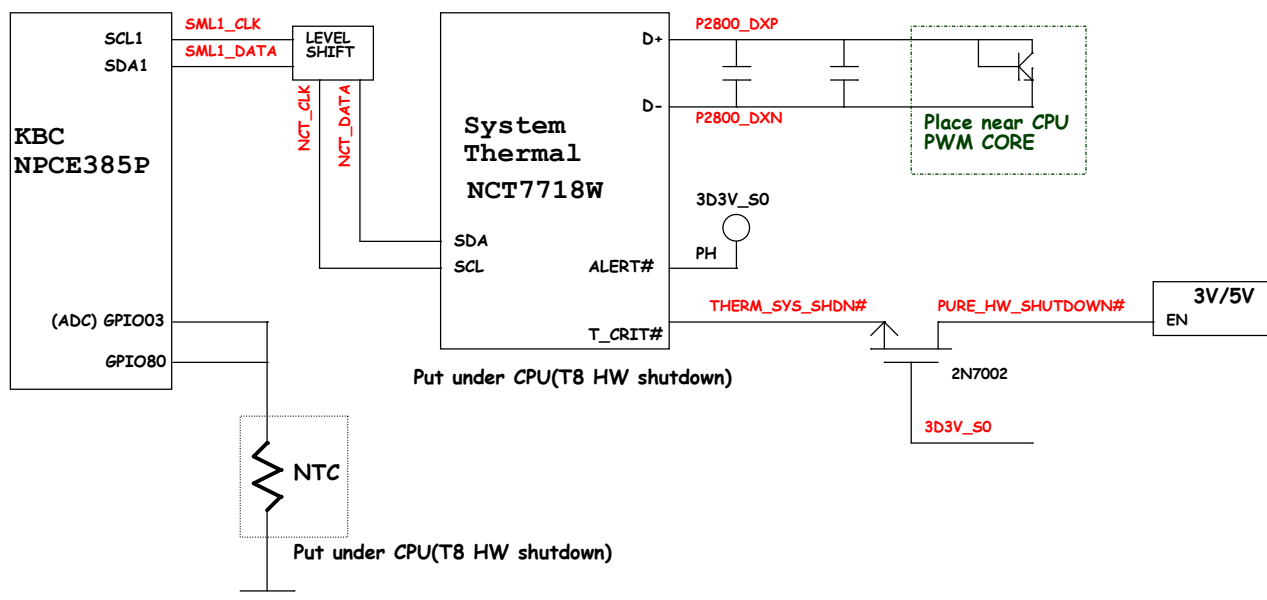
Parameter	Max	Typical	Min	Description
T1			10ms	From S5 power rails to RSMRST_L.
T2	16.5ms			From RSMRST_L to RTCCLK. *This timing is only valid if a Schmitt trigger is used or RC time constant of 10ms is used.
T3	138us		106us	From PWR_BTN_L/AGPIO0(falling) to SLP_S3_L(rising) and SLP_S5_L(rising).
T5			1ms	From power rails stable to PWR_GOOD (rising).
T8	16ms		15ms	From PWR_GOOD (rising) to PCIE_RST_L/EGPIO126(rising).
T9	20ms		12ms	From PWR_GOOD (rising) to clock (GFX_CLKP/N, GPP_CLKP [0-3], and GPP_CLKN[0-3]) stable.

<Variant Name>

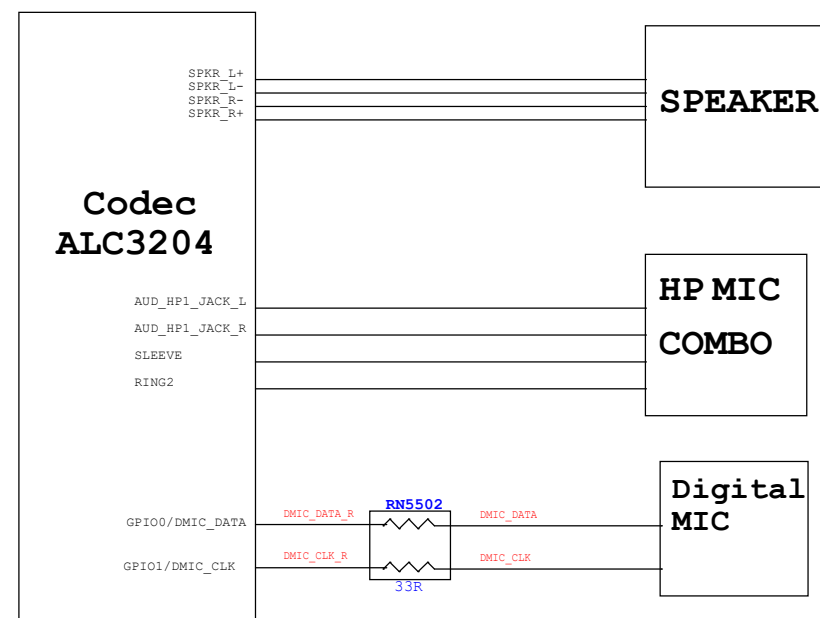


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Thermal Block Diagram




Audio Block Diagram



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CLK / USB Block

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DELL

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